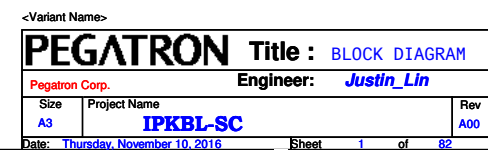


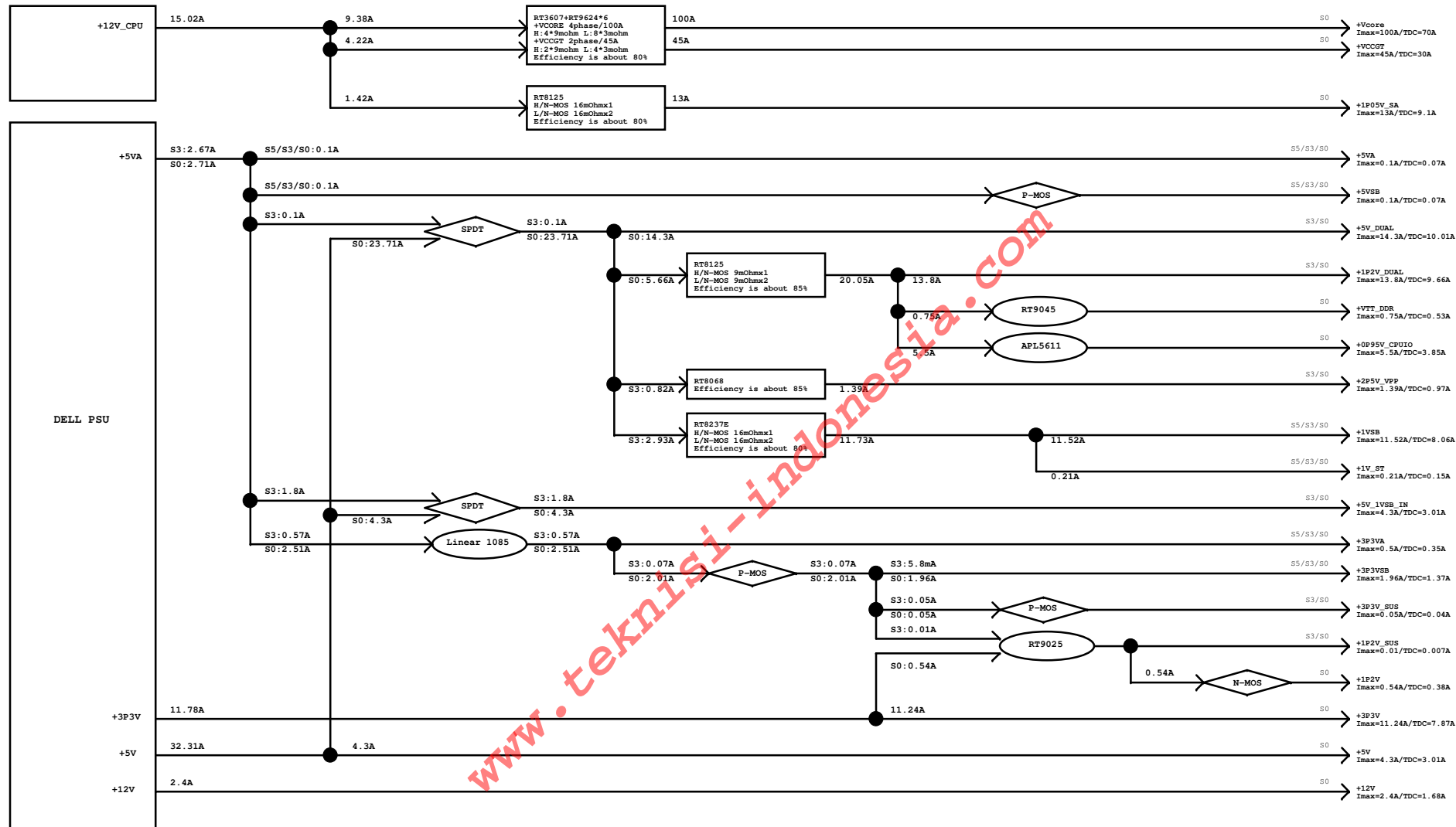
Revision: A00

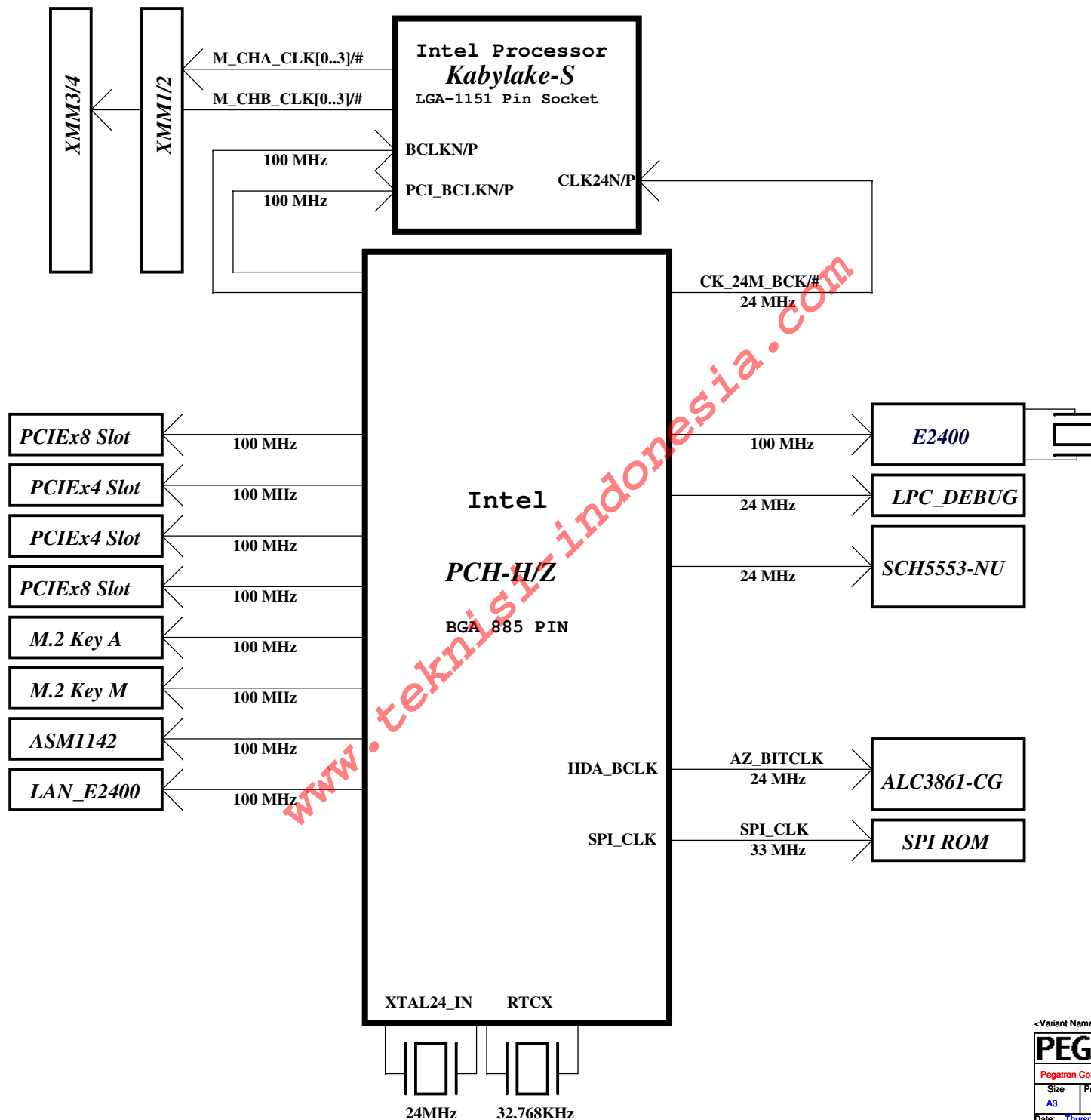
79	REAR USB 2.0 X4 CONN
80	USB CHARGE
81	REAR AUDIO CONN
82	LED DRIVER



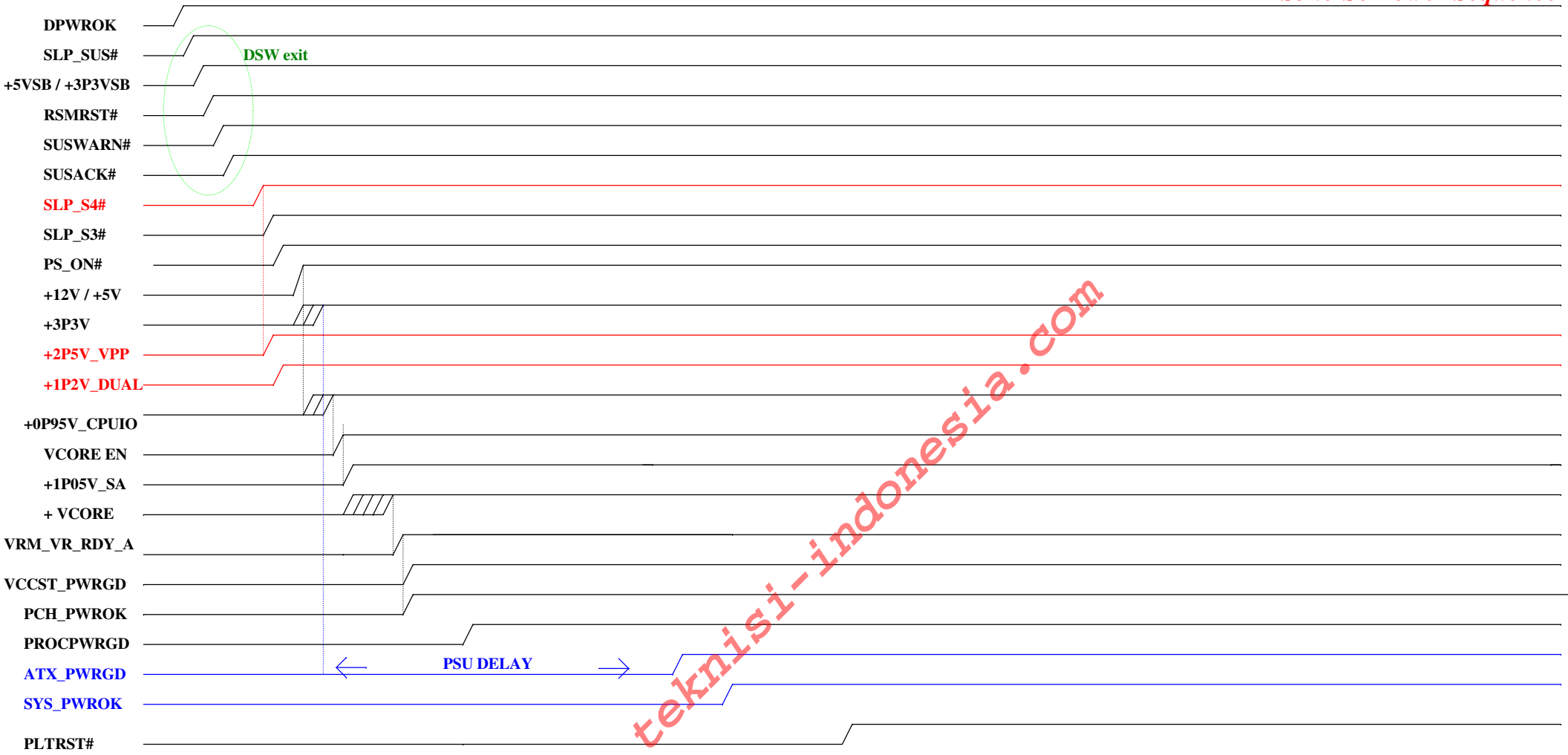
Schematics Change History

Version	Date	Page	Comments
X00	2016/07/12	36	Add 2.2 uF MLCC cap for ASMEDIA requirement (UC91,UC92)
X00	2016/07/13	18	Change SR1, SR2 to 1K pull down for Intel requirment
X01	2016/09/20	39	J_TYPEC (NBR2D-AK1320 to NBR2D-AK1322) for improving the SMT assembly yield rate for the mass production at factory side
X01	2016/09/20	29	Refer to CRB design to update XDP schematic (SR7622)
X01	2016/09/20	20	Adjust SR83 and SR84 from 0 ohm to 22 ohm for LPC EA issue
X01	2016/09/21	23	Adjust capacitance (SC8=SC9=12PF) for 24M Crystal optimization
X01	2016/09/21	23	Adjust capacitance (SC6=SC7=15PF) for 32.768K Crystal optimization
X01	2016/09/21	60	PR124=39.2KΩ; PC15=2.2uF for sequence tCPU05
X01	2016/09/22	All	PEGA sourcer strategy, most caps are modified as 0201 size except critical signal (HSIO)
X01	2016/09/29	43, 44	Change capacitance from Electrolytic type (CE3, CE4, UCE8) to MLCC type (UC10, UC11, UC15, UC13, UC14, UC16, UC966, UC967, UC968) to avoid M.2 interference
X01	2016/09/29	48	Modify SCB75 from 10pF/50V to 180pF/50V for Reset EA issue.
X01	2016/10/04	80	Fixed power Leakage of GPP_E9/E10/E11 and GPP_C16, add UR69731 and UR69732 to +5V_DUAL.
X01	2016/10/04	61	Reserve footprint (P1CB13, P1CB14, P1CB15, P1CB16) for EMI requirement.
X01	2016/10/06	11	Follow Intel CRB circuit 1.0, change the TP_VCC_OPC_1P8, TP_VCCOPC, TP_VCCEOPO and N22873652 to GND
X01	2016/10/11	19	Update Board ID to 101
A00	2016/11/14	11	Reference PDG, add a resistor 56 ohm connected to VCCST_PWRGD
A00	2016/11/14	46	Optimized the circuit, remove AXU_CH_P pull- up resistor M1R9 and AXU_CH_N pull-down resistor M1R10
A00	2016/11/14	19	Update Board ID to 110





S5 to S0 Power Sequence



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	CPU KabyLake-S 42 K-SKU
+VCORE	-> 100A (Imax)
+0P95V_CPUIO	-> 5.5A (Imax)
+1P05V_SA	-> 11.1A (Imax)
+V_AXG	-> 45A (Imax)

	PCH
+1VSB	-> 7.858A
+3P3V	-> 0.007A
+3P3VSB	-> 0.78A
+3P3VA	-> 0.20A
+BATT	RTC(G3) -> 6uA

	DDR4-2400(4) & Termination
+1P2V_DUAL	-> 10.8A
+VPP(2.5V)	-> 1.12A
+VTT_DDR(0.75V)	-> 0.53A

	PCI Express x 16 (75W)
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

	PCI Express x 4 (25W)
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 4 (25W)
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 16 (75W)
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

	REAR USB2.0 6 PORTS
+5V_DUAL	->3A

	REAR USB3.0 4 PORTS
+5V_DUAL	->4.5A

	M.2 SSD / M.2 WIFI
+3P3V	-> 0.9A / 0.6A

	Killer E2400
+3P3VSB	-> 0.151A

	REAR TYPE C
+5V_DUAL	->3A

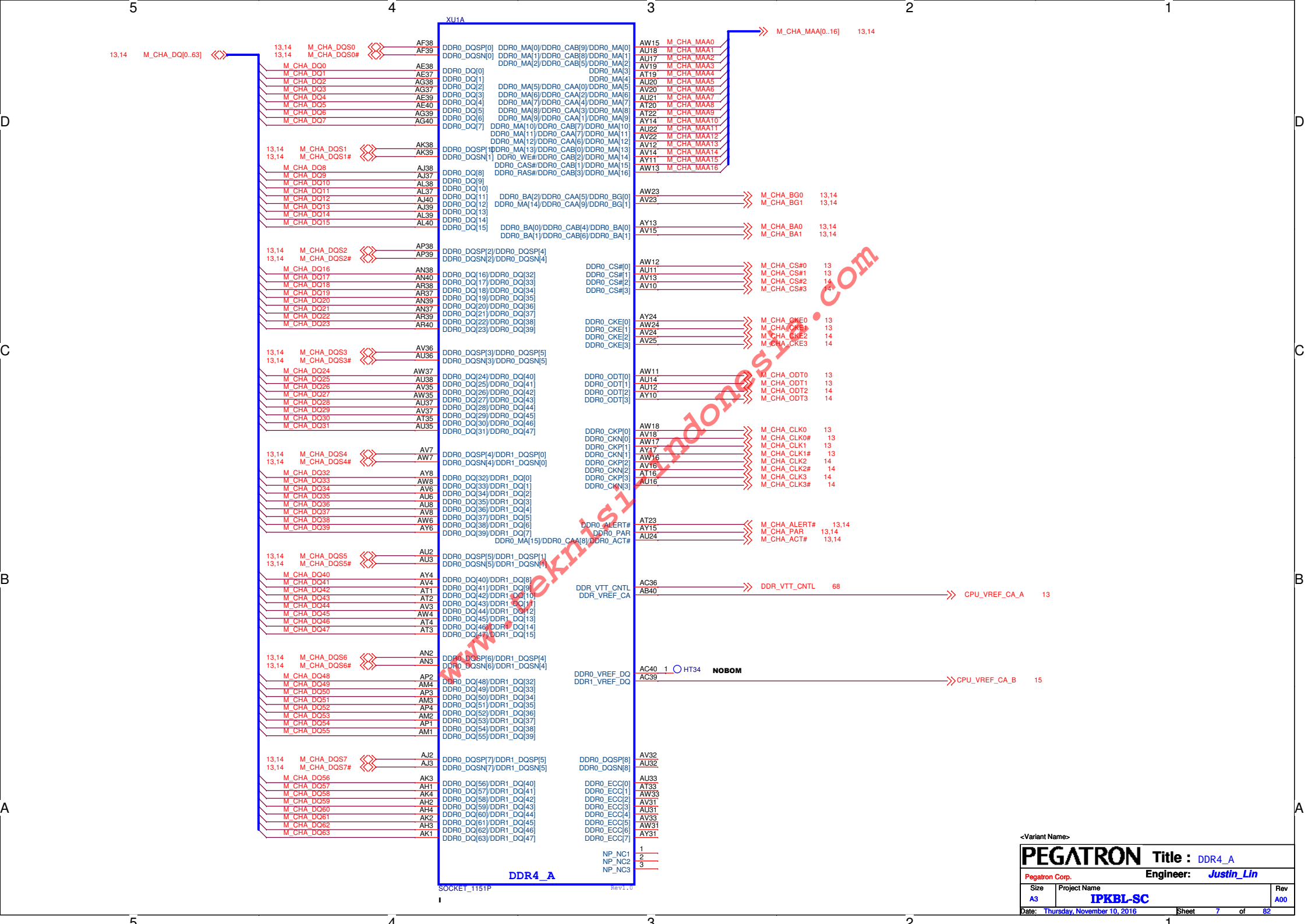
	TOP FAN
+12V_CPU	-> 0.8A

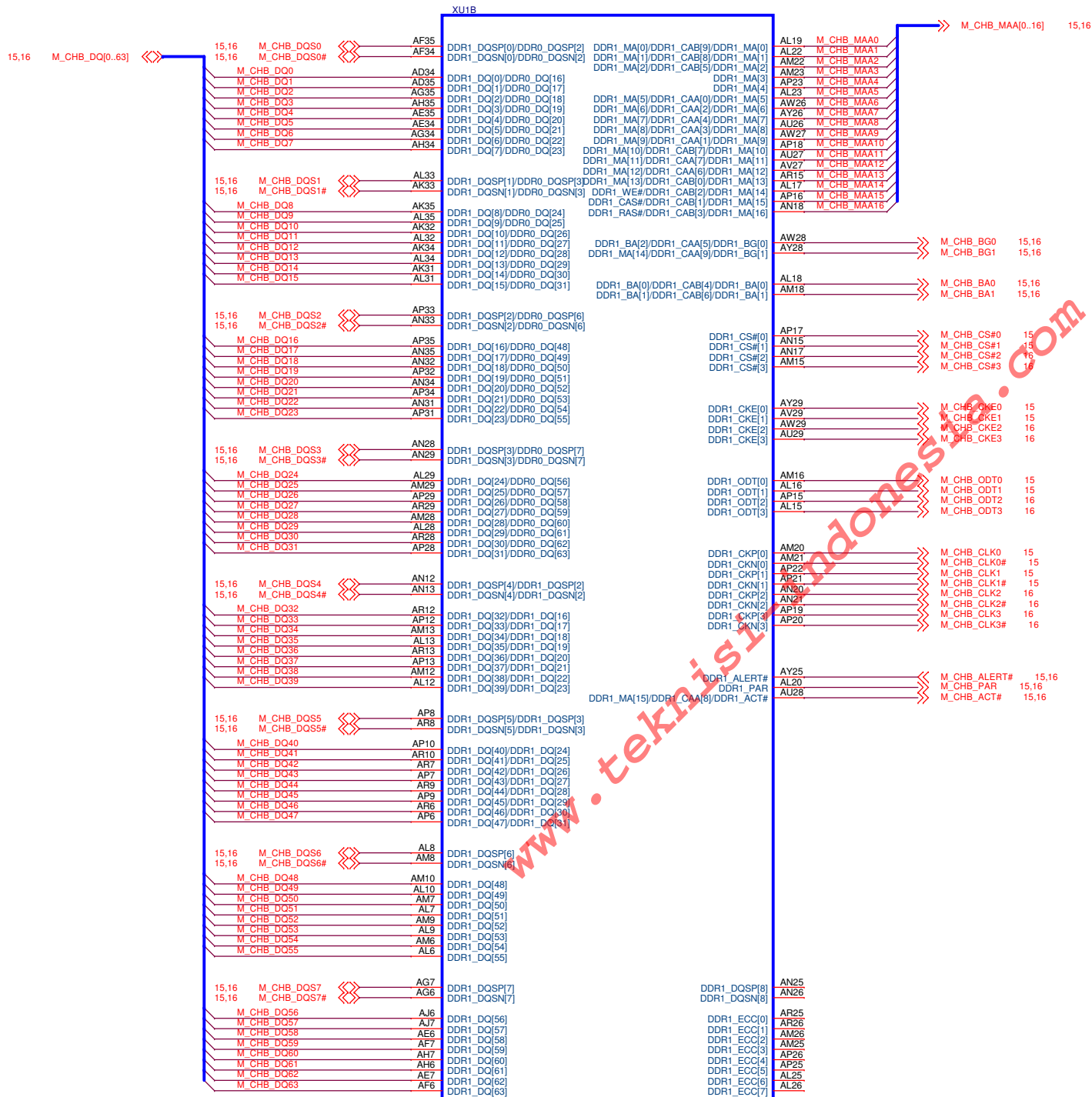
	PUMP/CPU FAN
+12V_CPU	-> 0.208A / 0.7A

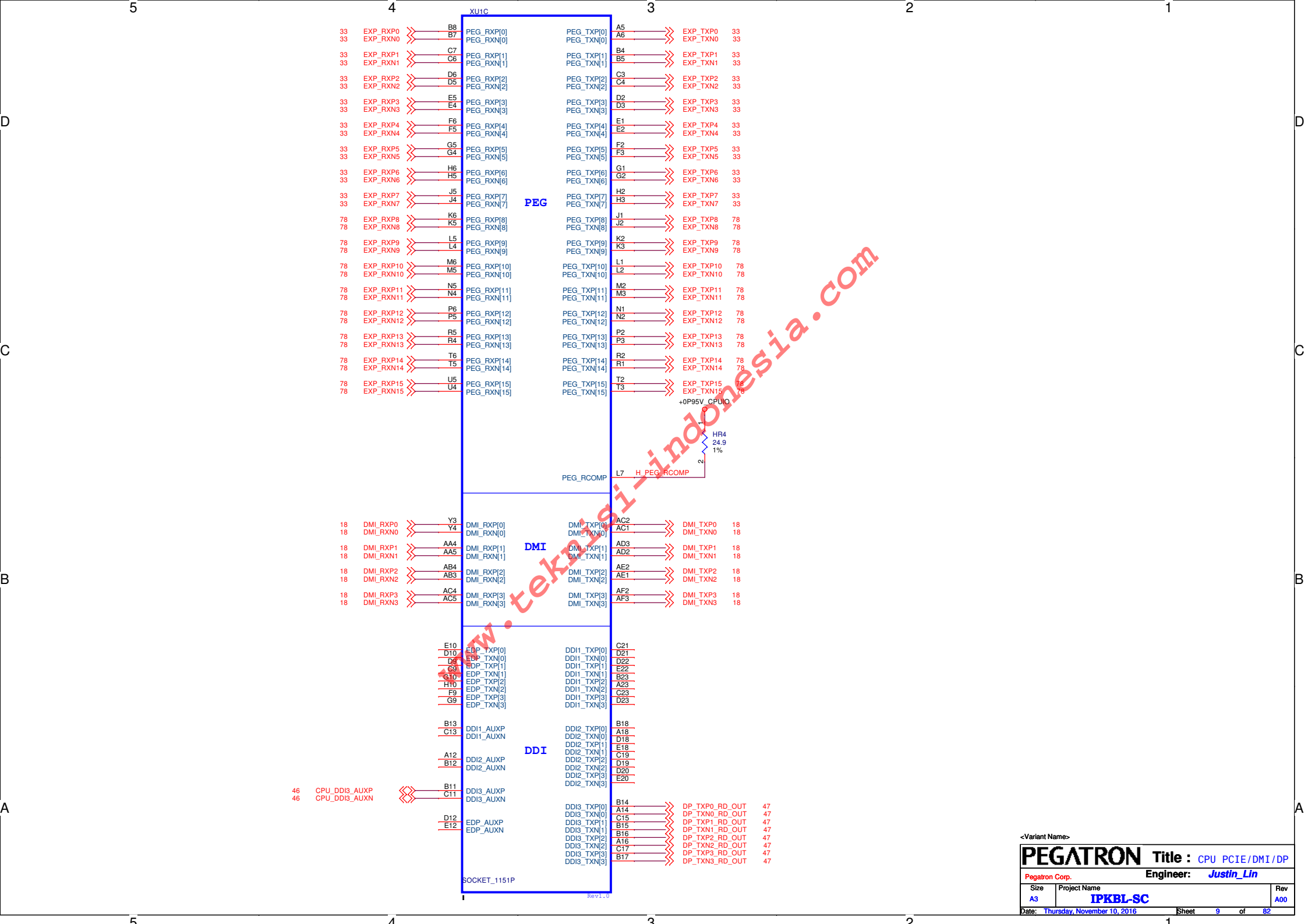
	GFX FAN
+12V_CPU	-> 0.8A

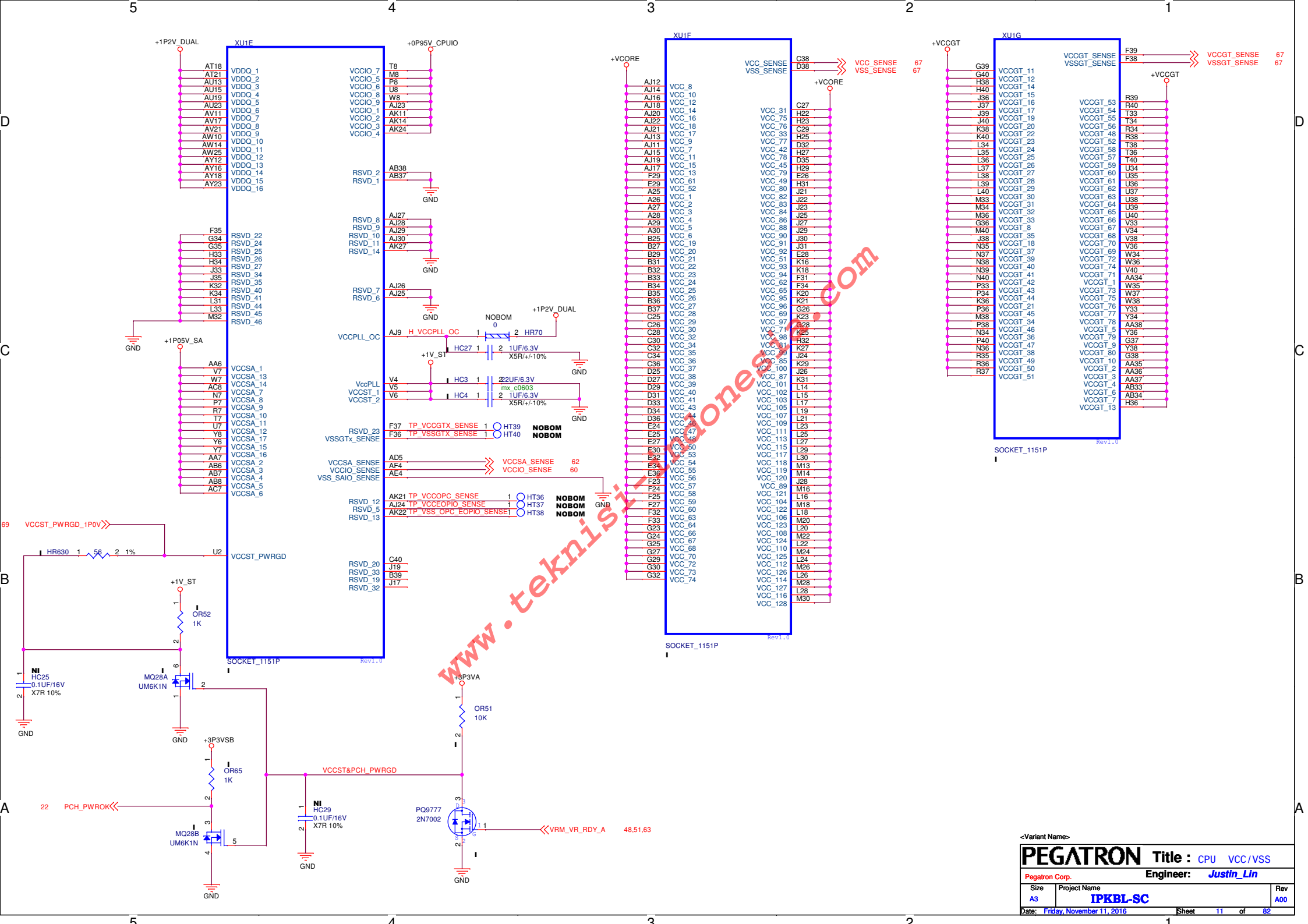
	FRONT USB3.0 2 PORTS
+5V_DUAL	->1A

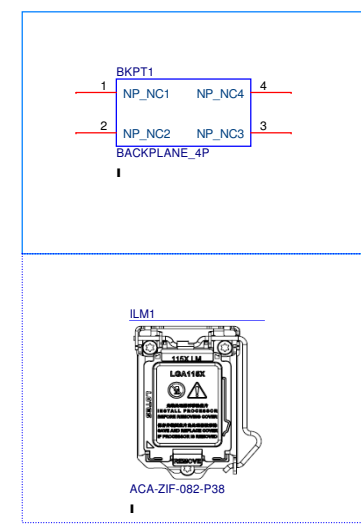
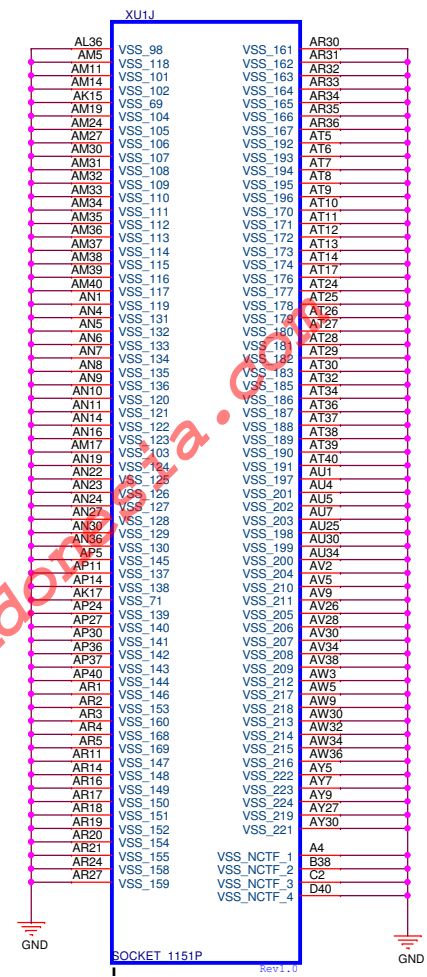
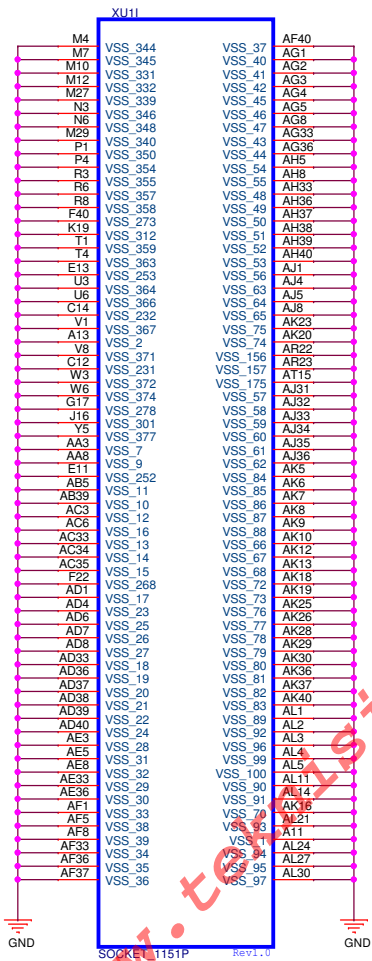
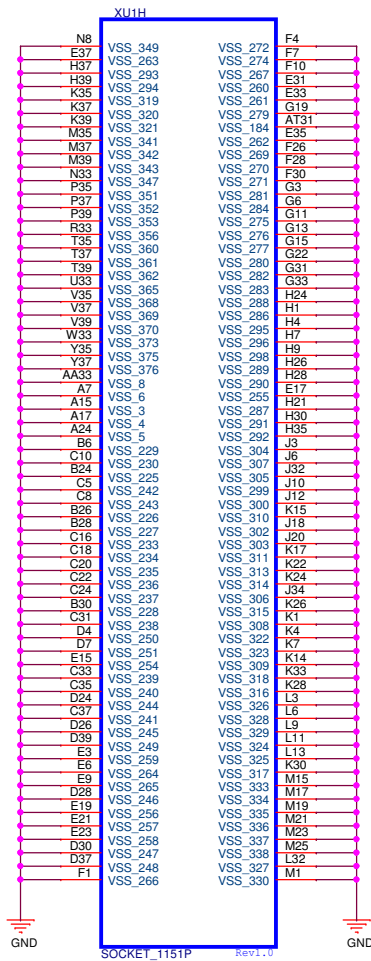
	FRONT USB3.0 2 PORTS Charge
+5V_1VSB_IN	->2.8A

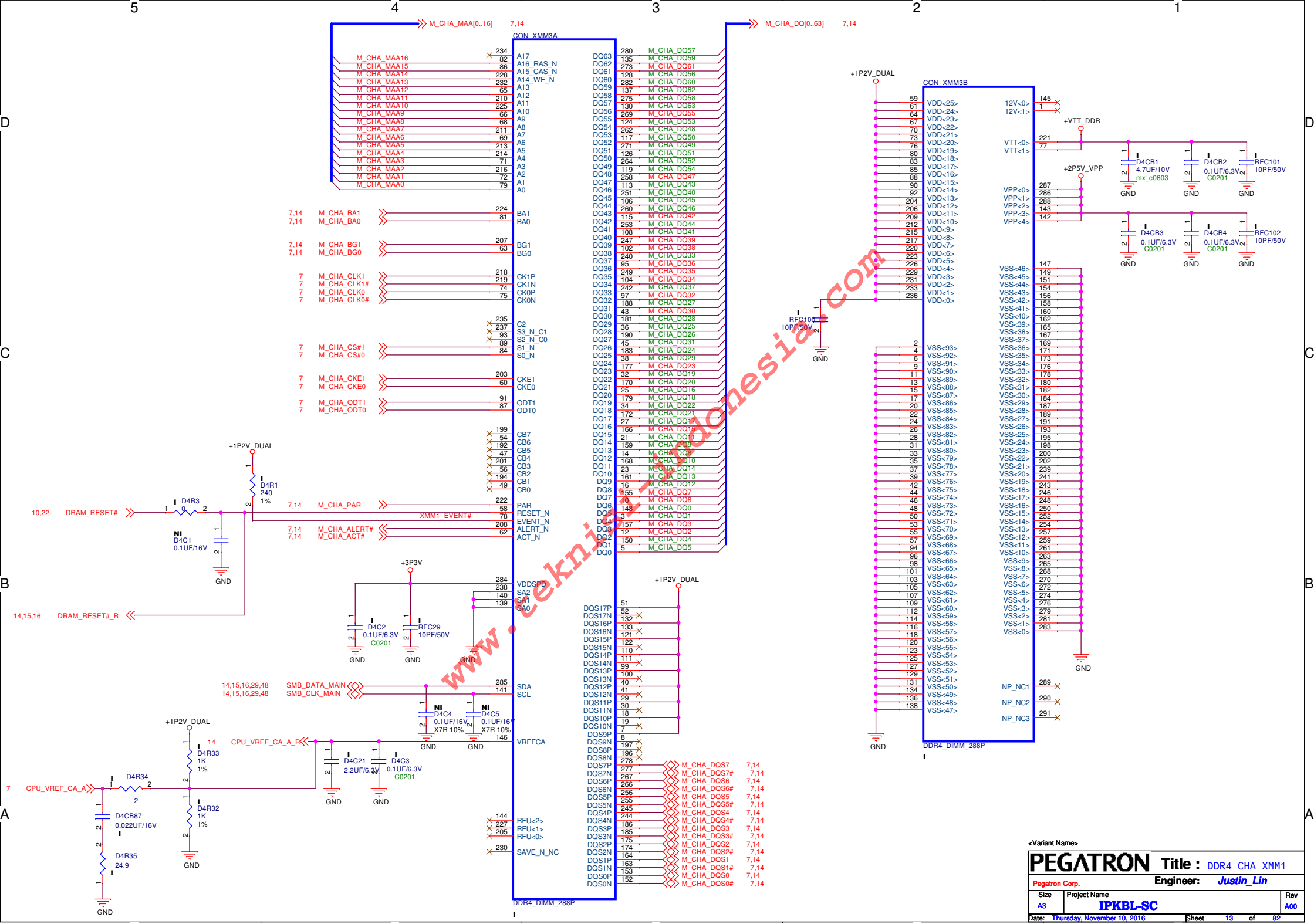


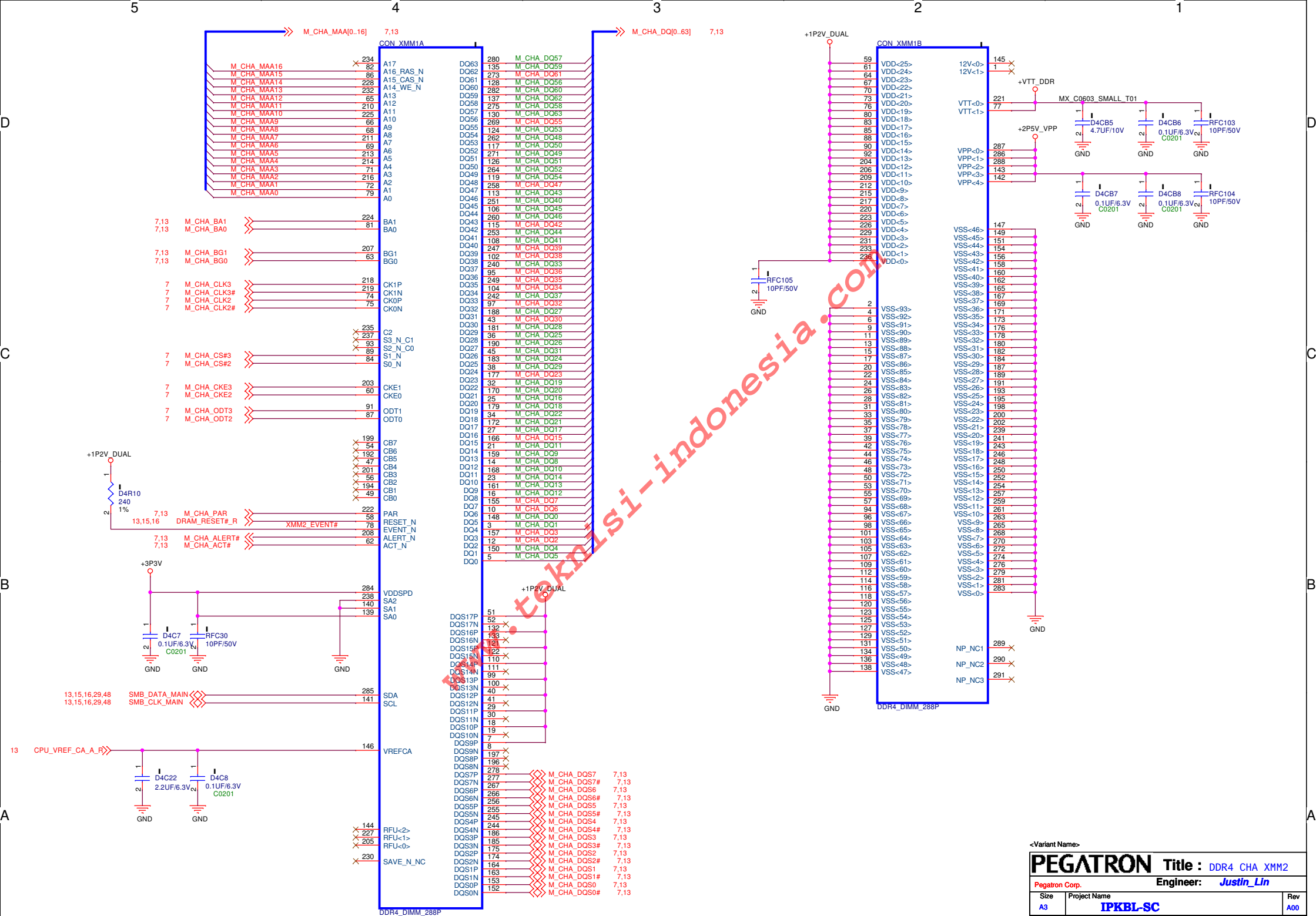


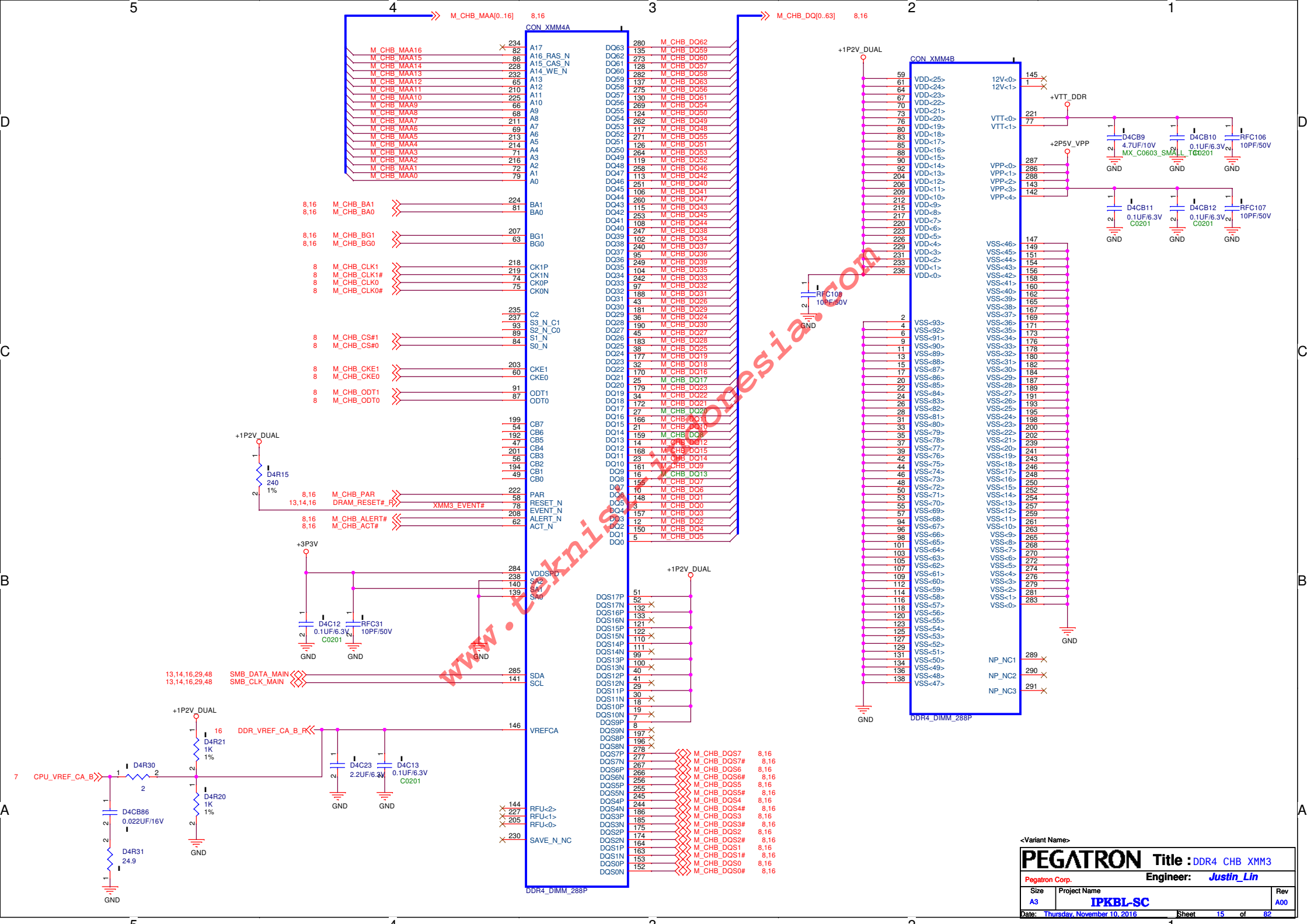


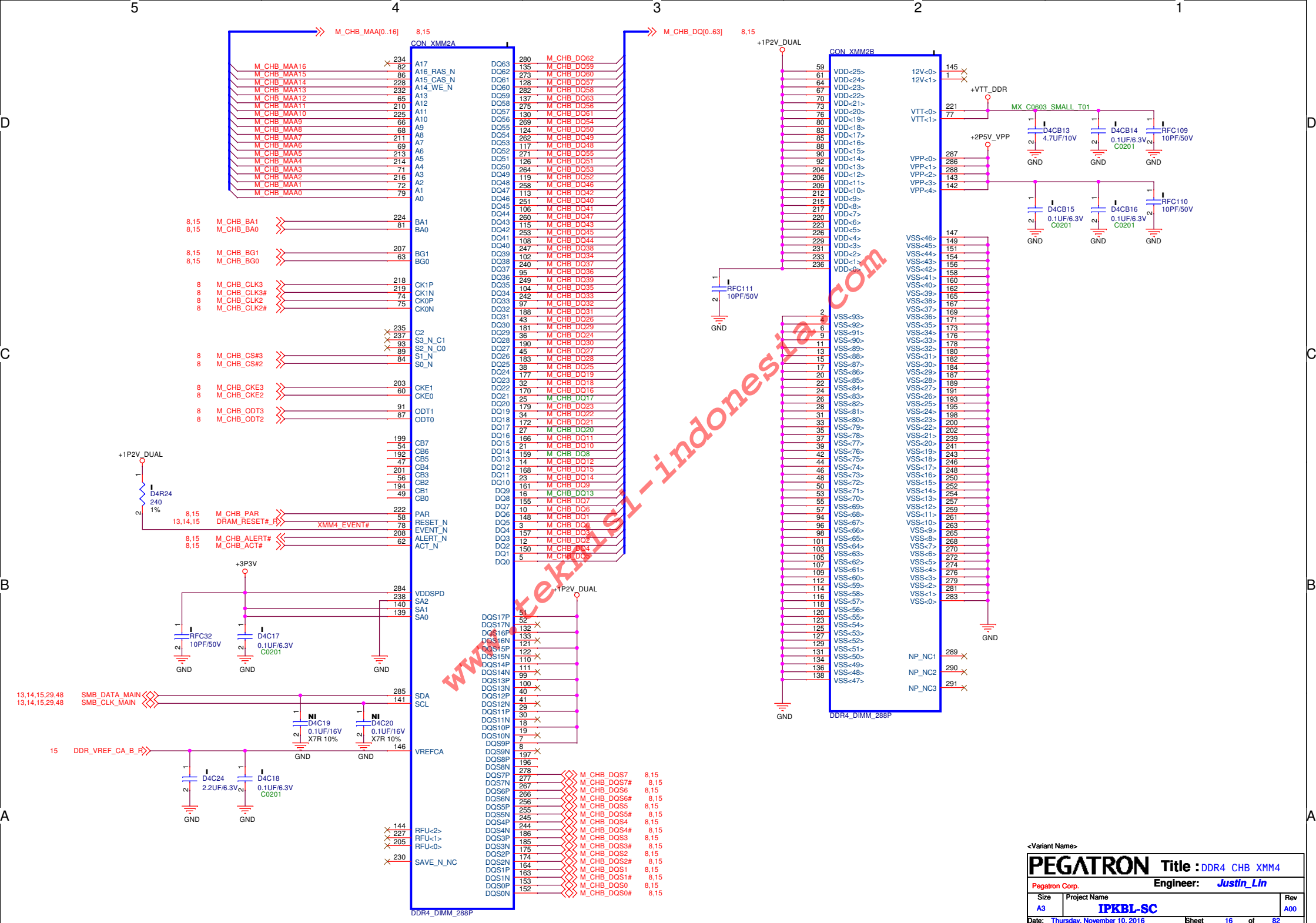














SATA HDD1

SATA HDD2

SATA HDD3

SATA HDD4

M.2 Key M slot

45 SATA_TXP0
45 SATA_TXN0
45 SATA_RXP0
45 SATA_RXN0

45 SATA_TXP1
45 SATA_TXN1
45 SATA_RXP1
45 SATA_RXN1

45 SATA_TXP2
45 SATA_TXN2
45 SATA_RXP2
45 SATA_RXN2

45 SATA_TXP3
45 SATA_TXN3
45 SATA_RXP3
45 SATA_RXN3

32 PE17_TXP
32 PE17_TXN
32 PE17_RXP
32 PE17_RXN

32 PE18_TXP
32 PE18_TXN
32 PE18_RXP
32 PE18_RXN

32 PE19_TXP
32 PE19_TXN
32 PE19_RXP
32 PE19_RXN

32 PE20_TXP
32 PE20_TXN
32 PE20_RXP
32 PE20_RXN

PCHB

PCIE/SATA

B36
C36
E36
G36
PCIE13_TXP/SATA0B_TXP
PCIE13_TXN/SATA0B_TXN
PCIE13_RXP/SATA0B_RXP
PCIE13_RXN/SATA0B_RXN

B37
A37
G37
E37
PCIE14_TXP/SATA1B_TXP
PCIE14_TXN/SATA1B_TXN
PCIE14_RXP/SATA1B_RXP
PCIE14_RXN/SATA1B_RXN

B38
C38
C42
E41
PCIE15_TXP/SATA2_TXP
PCIE15_TXN/SATA2_TXN
PCIE15_RXP/SATA2_RXP
PCIE15_RXN/SATA2_RXN

A39
B39
E43
D42
PCIE16_TXP/SATA3_TXP
PCIE16_TXN/SATA3_TXN
PCIE16_RXP/SATA3_RXP
PCIE16_RXN/SATA3_RXN

F45
E45
K39
J41
PCIE17_TXP/SATA4_TXP
PCIE17_TXN/SATA4_TXN
PCIE17_RXP/SATA4_RXP
PCIE17_RXN/SATA4_RXN

G44
G45
M41
M39
PCIE18_TXP/SATA5_TXP
PCIE18_TXN/SATA5_TXN
PCIE18_RXP/SATA5_RXP
PCIE18_RXN/SATA5_RXN

H45
H44
P41
P39
PCIE19_TXP/SATA6_TXP
PCIE19_TXN/SATA6_TXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN

J44
J43
P36
P38
PCIE20_TXP/SATA7_TXP
PCIE20_TXN/SATA7_TXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN

K44
K43
T41
T39
PCIE_21_TXP
PCIE_21_TXN
PCIE_21_RXP
PCIE_21_RXN

L44
L43
V36
V35
PCIE_22_TXP
PCIE_22_TXN
PCIE_22_RXP
PCIE_22_RXN

N45
N44
V41
V39
PCIE_23_TXP
PCIE_23_TXN
PCIE_23_RXP
PCIE_23_RXN

P44
P43
Y41
Y39
PCIE_24_TXP
PCIE_24_TXN
PCIE_24_RXP
PCIE_24_RXN

AF44
AG41
AH39
AH36
AF45
GPP_F9/DEVSLP3
GPP_F6/DEVSLP4
GPP_F7/DEVSLP5
GPP_F8/DEVSLP6
GPP_F9/DEVSLP7

AE30
AH35
AE44
AE43
AD44
GPP_F10/SCLK
GPP_F11/SLOAD
GPP_F12/SDATAOUT1
GPP_F13/SDATAOUT0
GPP_F14

AC42
AE35
AE36
GPP_F19/6DP_VDDEN
GPP_F20/6DP_BKLTEN
GPP_F21/6DP_BKLTCTL

AB45
AE39
GPP_F22
GPP_F23

GPP_E0/SATAxPCIE0/SATAGP0
GPP_E1/SATAxPCIE1/SATAGP1
GPP_E2/SATAxPCIE2/SATAGP2

GPP_E3/CPU_GP0
GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2
GPP_E7/CPU_GP1
GPP_E8/SATALED#

GPP_E9/USB_OC0#
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GPP_E11/USB_OC2#
GPP_E12/USB_OC3#
GPP_F15/USB_OCB4#
GPP_F16/USB_OCB5#
GPP_F17/USB_OCB6#
GPP_F18/USB_OC7#

GPP_I0/DDPB_HP0D
GPP_I1/DDPC_HP0D
GPP_I2/DDPD_HP0D
GPP_I3/DDPE_HP0D
GPP_I4/EDP_HP0D

GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA

GPP_F0/SATAxPCIE3/SATAGP3
GPP_F1/SATAxPCIE4/SATAGP4
GPP_F2/SATAxPCIE5/SATAGP5
GPP_F3/SATAxPCIE6/SATAGP6
GPP_F4/SATAxPCIE7/SATAGP7

AM36
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AM34

AP41
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AL45
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AK43
AJ44

AJ43
AH44
AM39
AK42

AD43
AC44
AH42
AC43

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AT8
AP8
AT7
BA1

AW5
AV7
AT5
BA6
AY1
AY2

AK36
AK33
AK38
AH43
AE42

+3P3VSB

SR129

10K

MF_MODE#_R

M2R48

1 0 2

MF_MODE# 71
HD_LED# 50

+3P3VSB

SR129

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+3P3VSB

SR129

10K

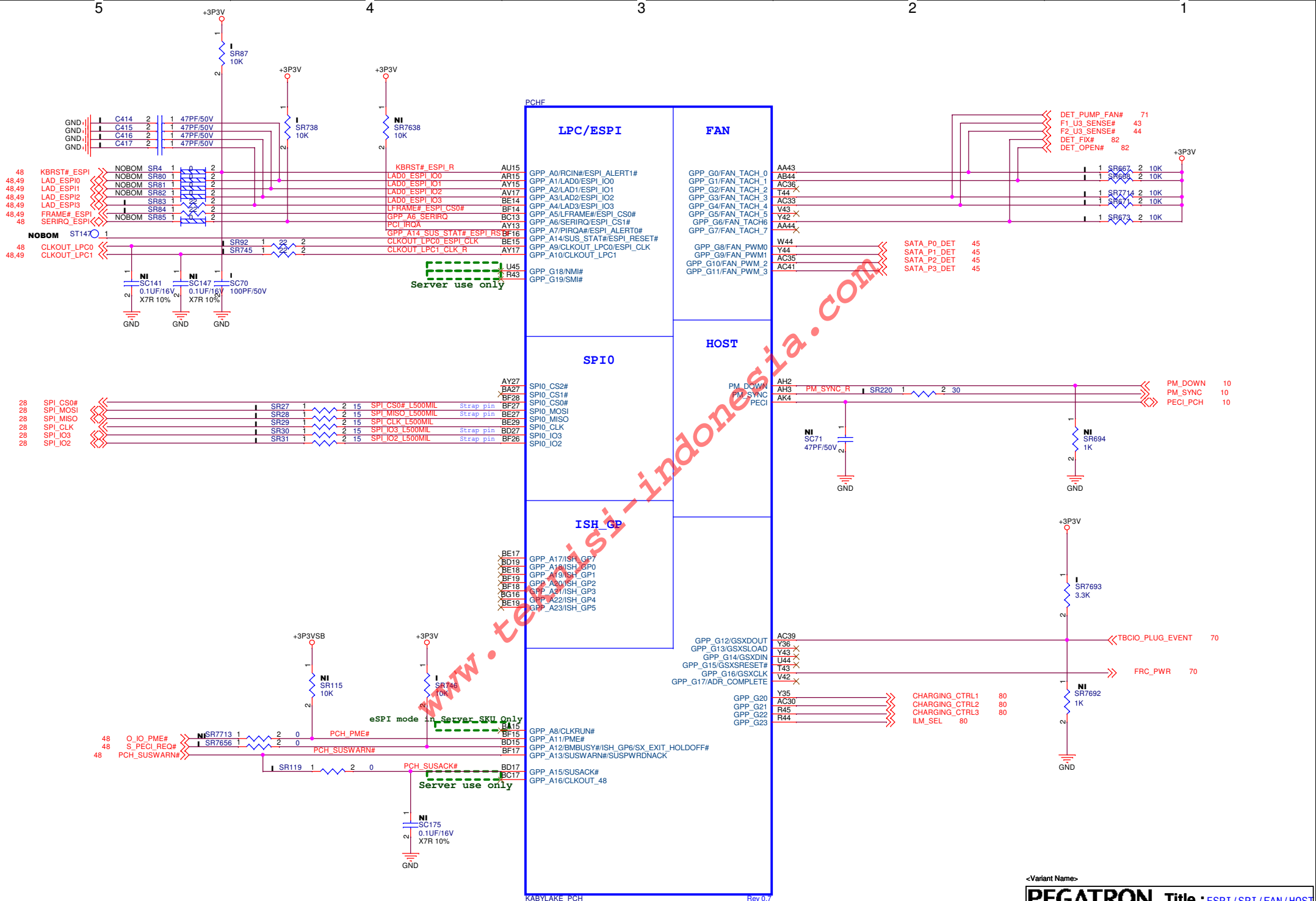
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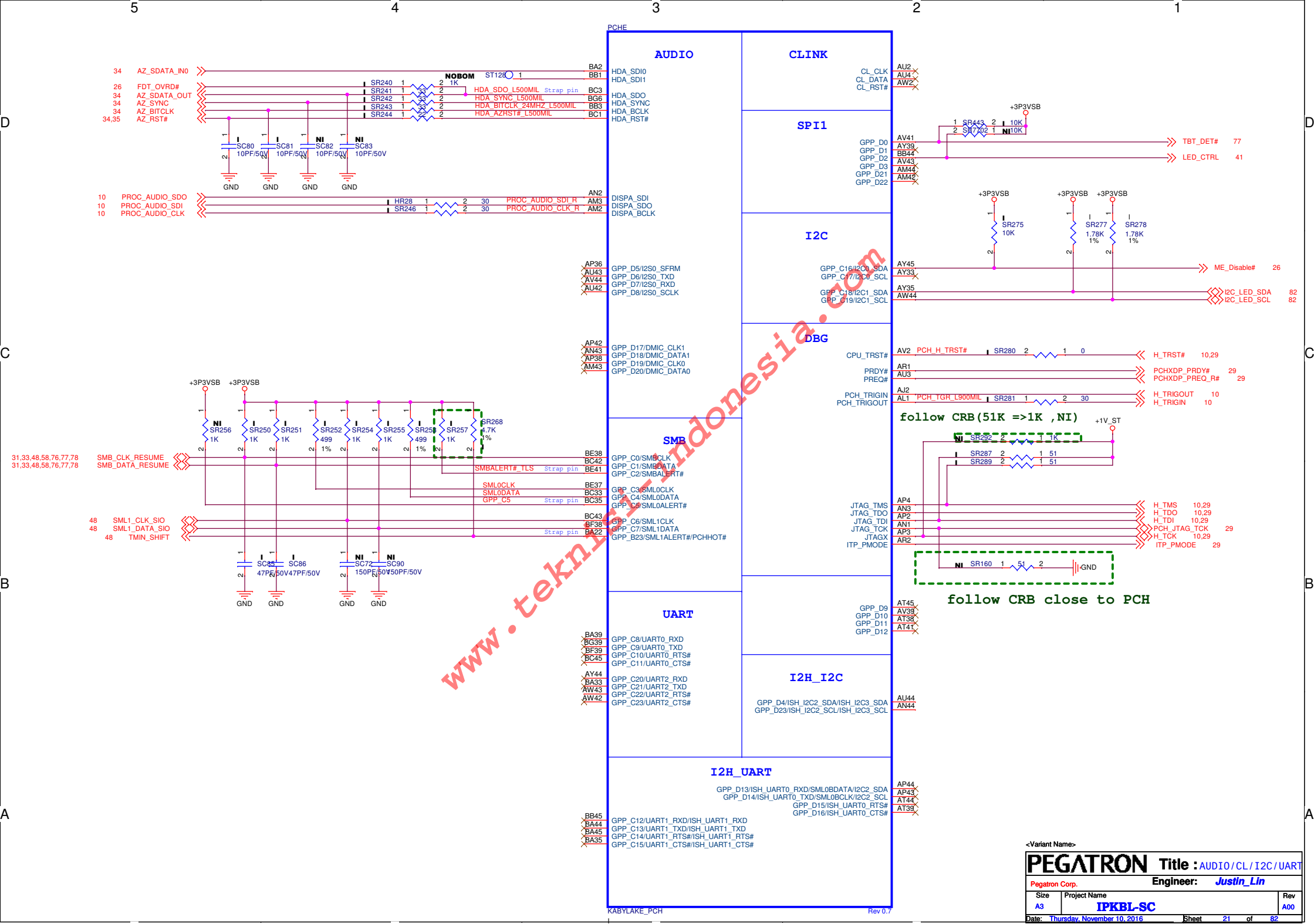
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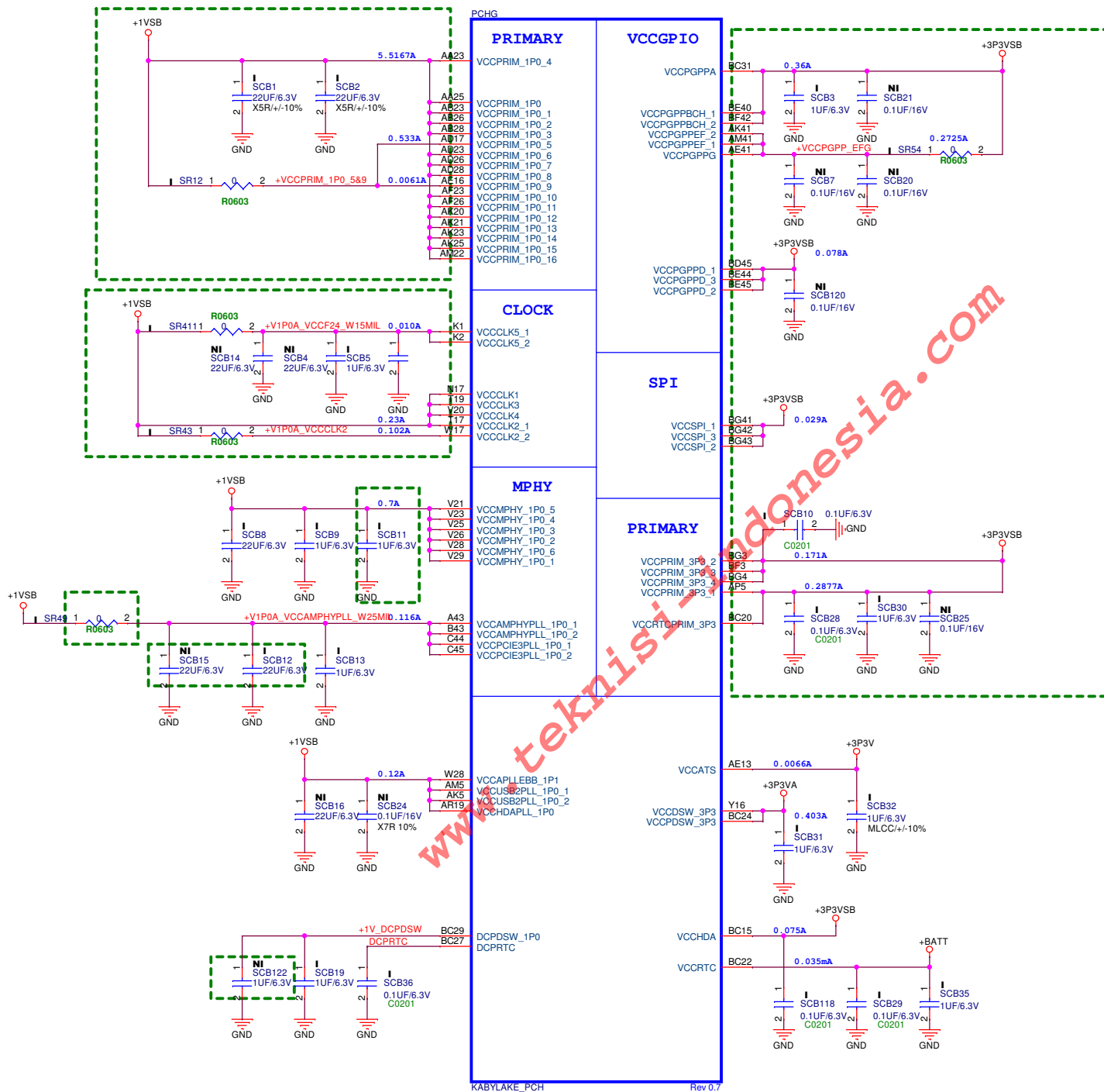
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+3P3V







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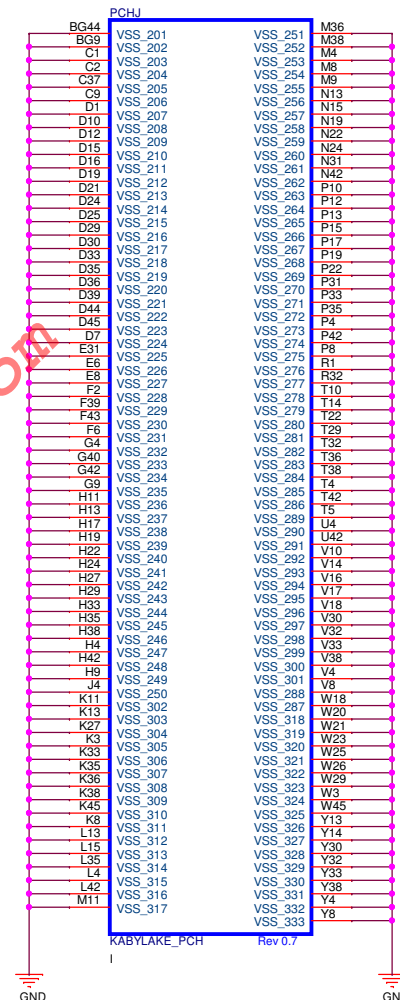
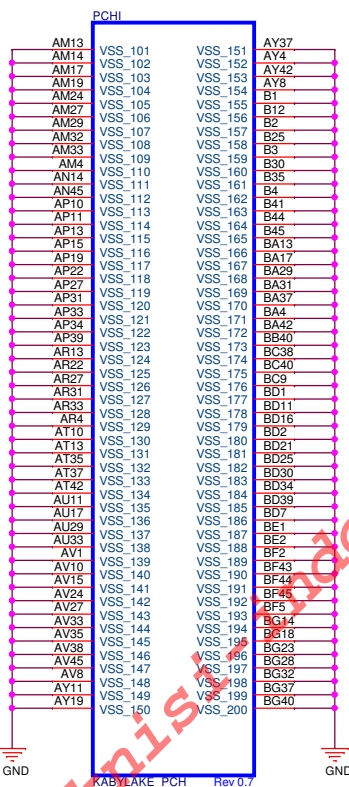
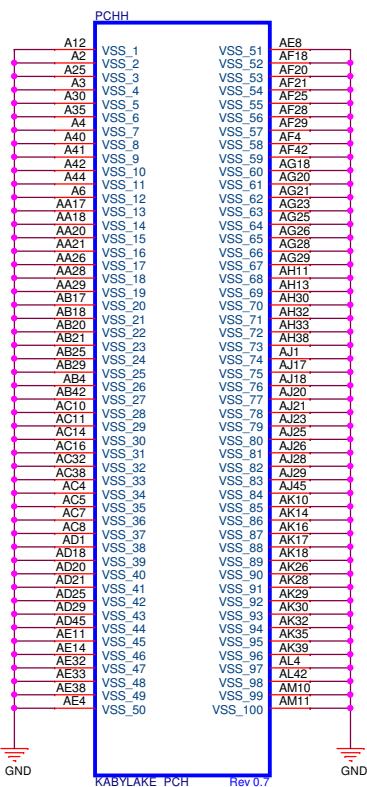
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Pegatron Corp. Engineer: Justin Lin

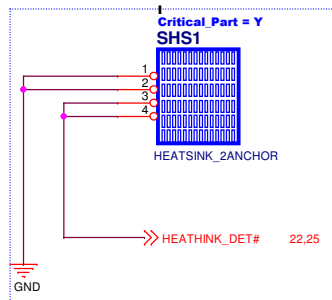
Size Project Name Rev

A3 IPKBL-SC A00

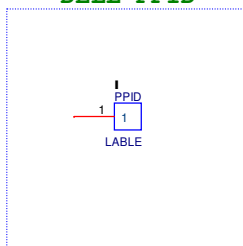
Date: Thursday, November 10, 2016 Sheet 24 of 84



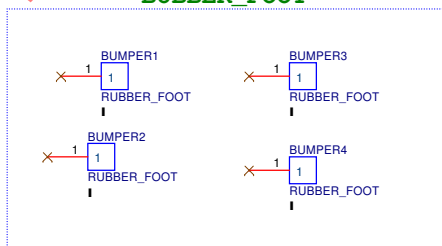
PCH Heatsinker



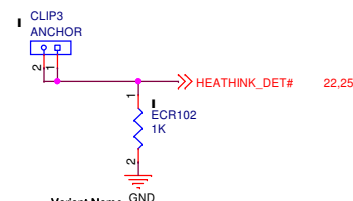
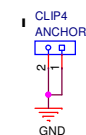
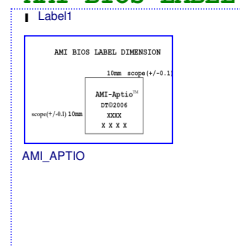
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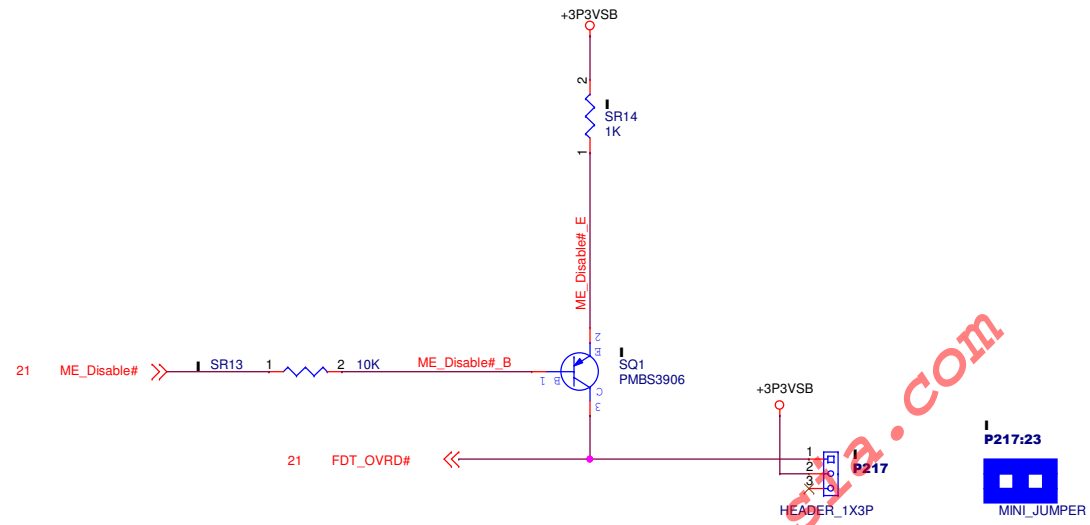


BUBBER_FOOT



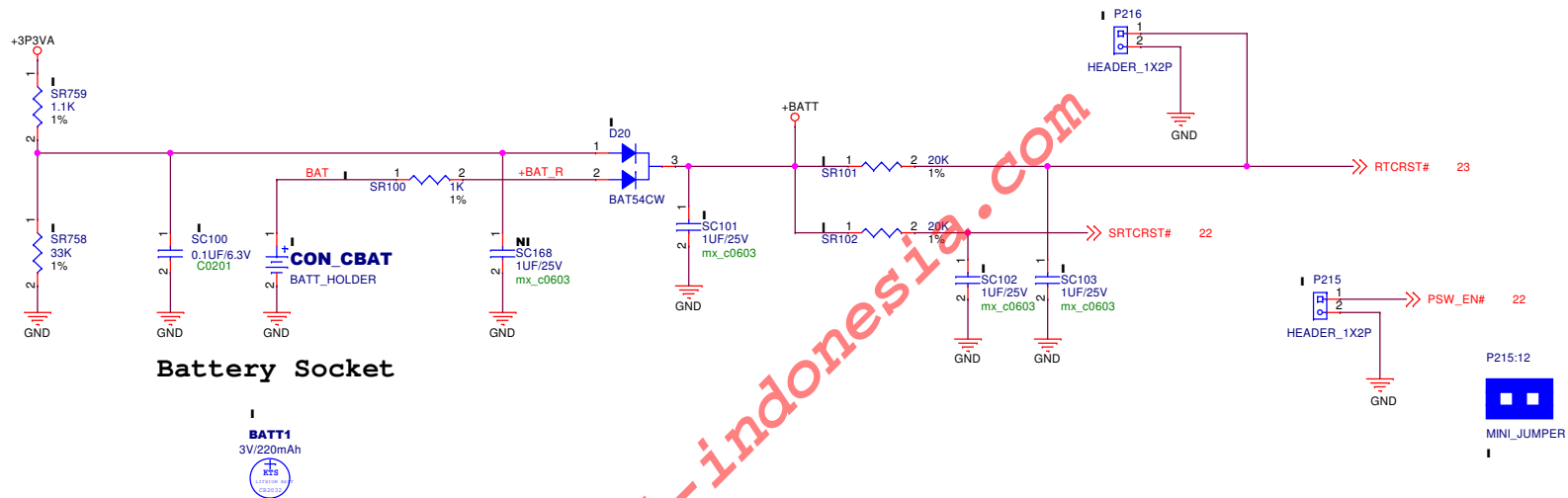
AMI BIOS LABEL





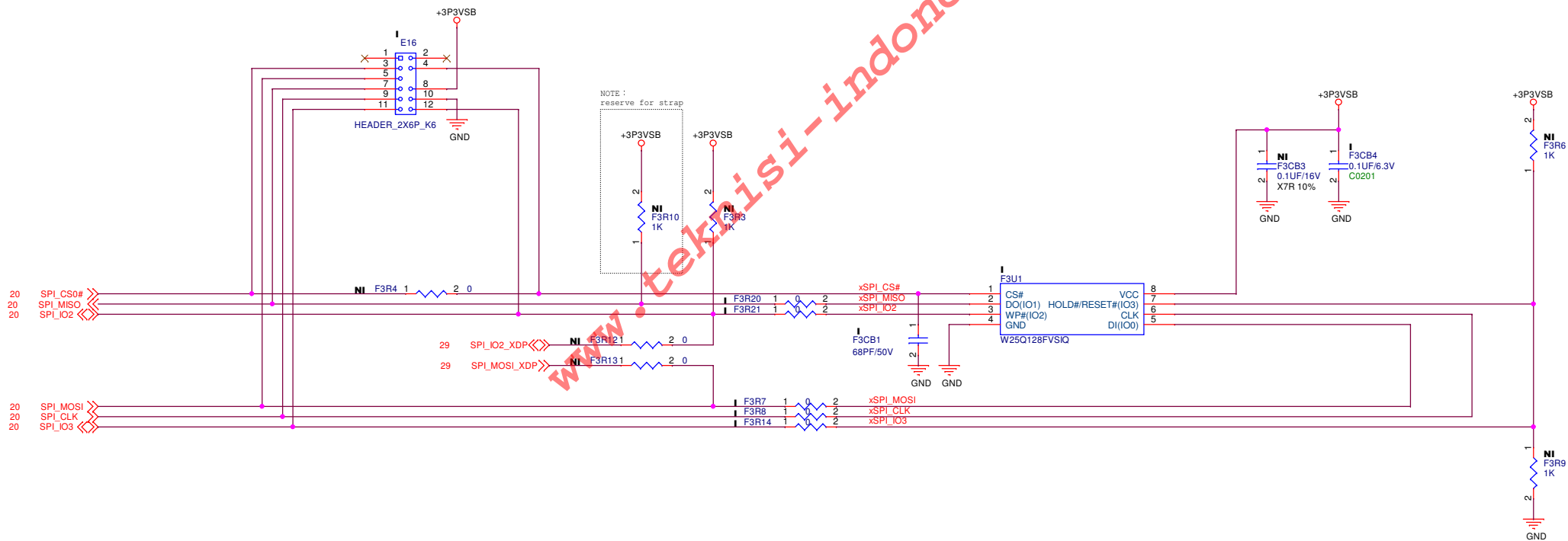
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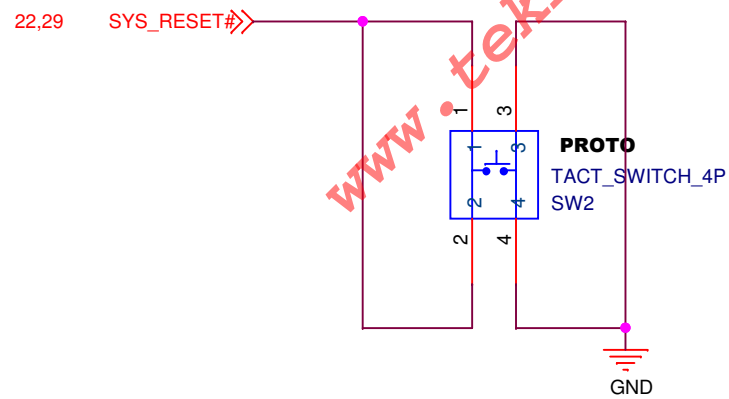
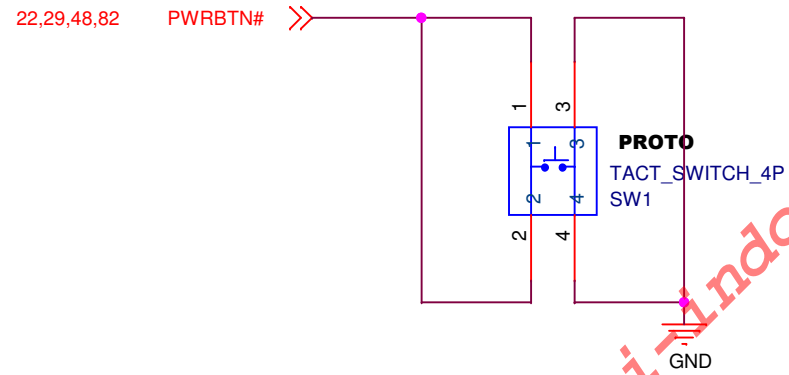
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PEGATRON		
Title : PCH_PLTRST		
Pegatron Corp.		
Engineer: Justin_Lin		
Size	Project Name	Rev
B	IPKBL-SC	A00
Date: Thursday, November 10, 2016		
Sheet 26 of 82		



<Variant Name>

PEGATRON		Title : RTC/CMOS	
Pegatron Corp.		Engineer: Justin_Lin	
Size A3	Project Name IPKBL-SC		Rev A00
Date: Thursday, November 10, 2016		Sheet 27 of 82	





<Variant Name>

Title

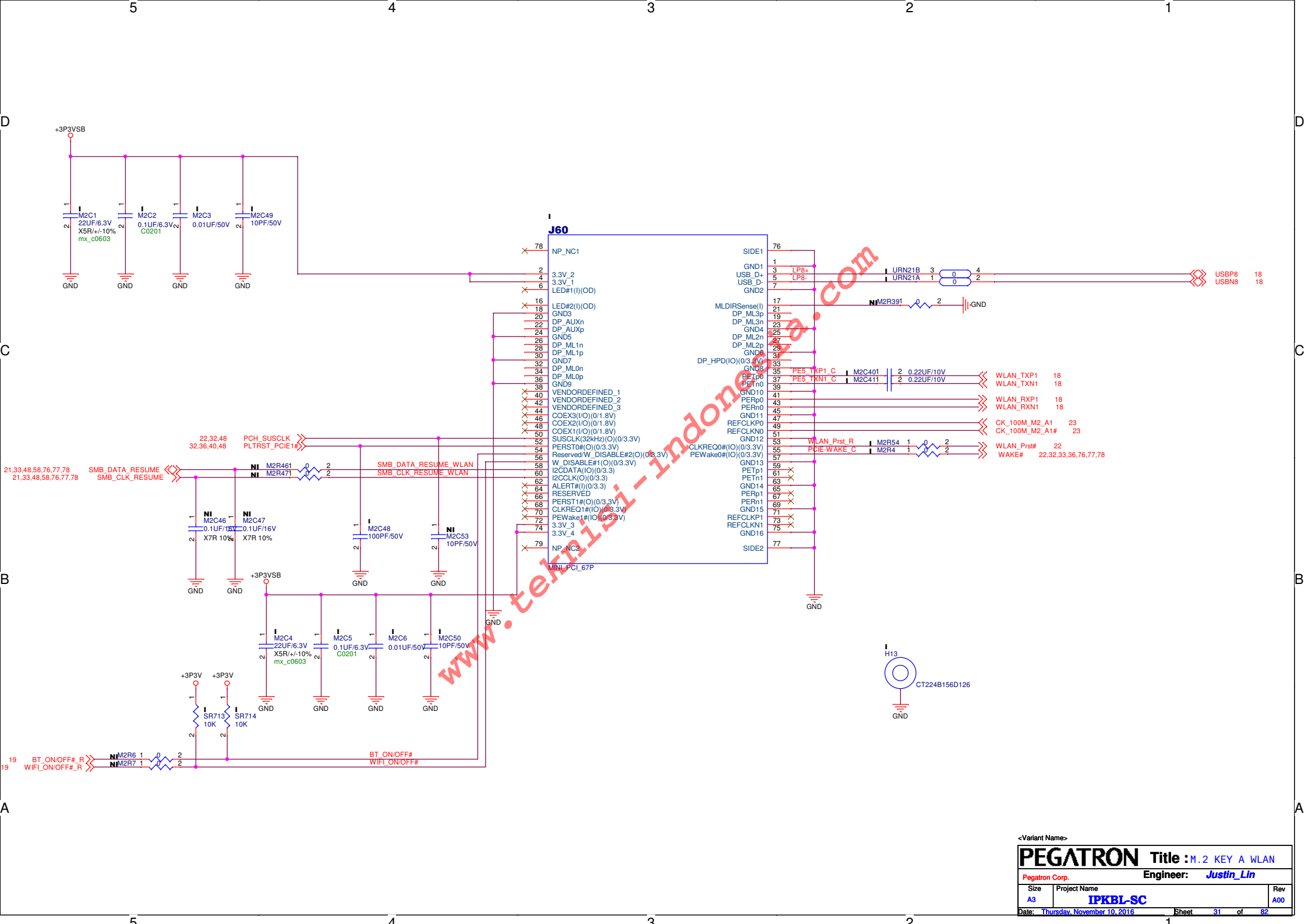
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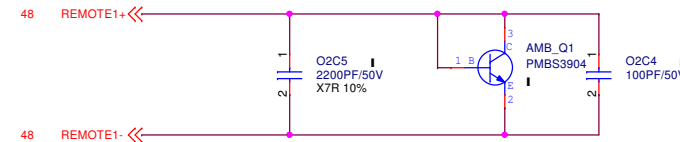
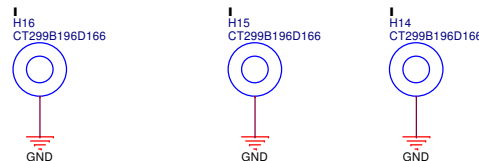
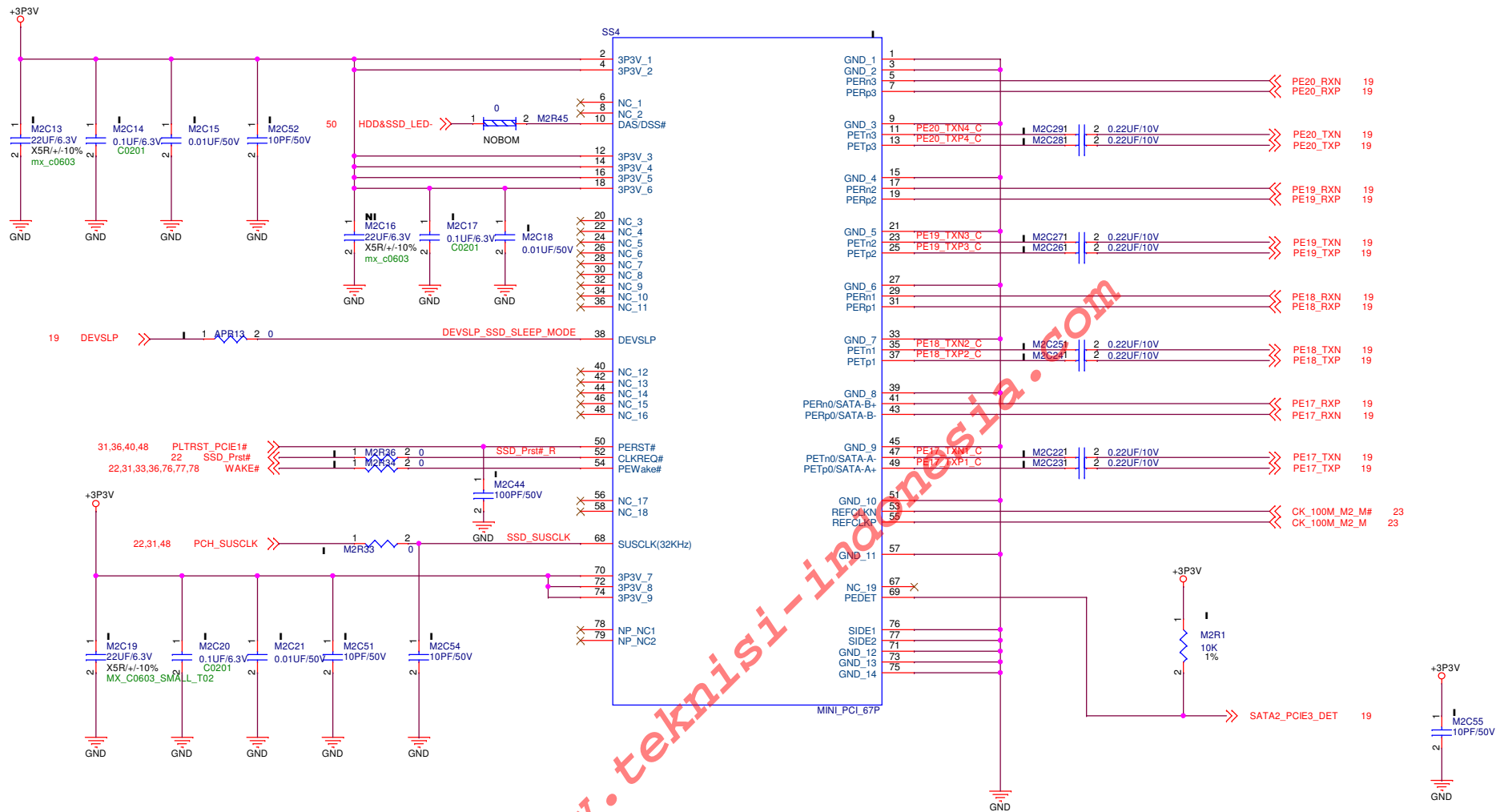
Size
A

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<Doc>

Rev
A00

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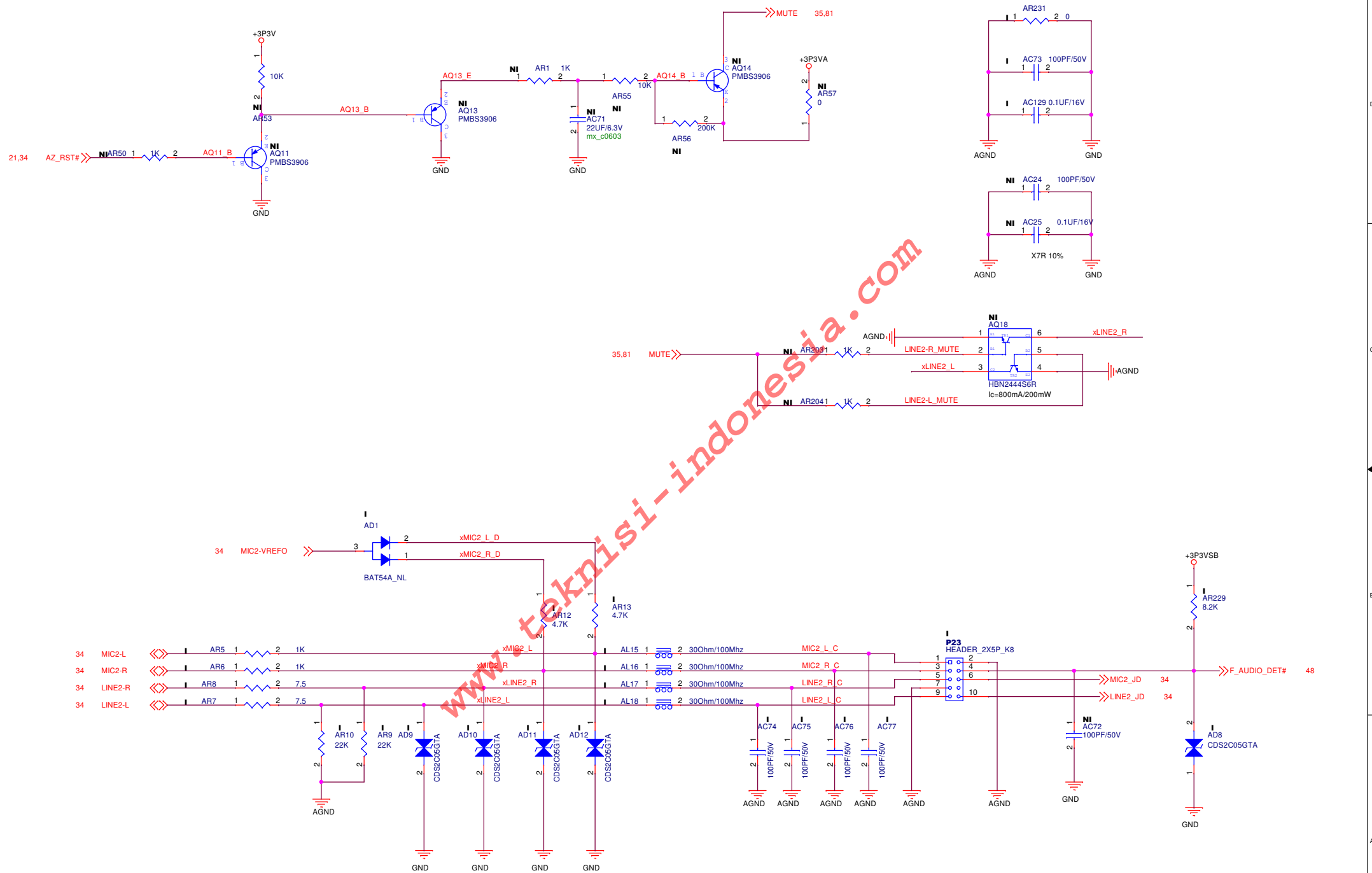
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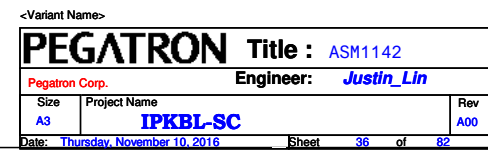
PEGATRON Title : M.2 KEY M SSD

Pegatron Corp. Engineer: Justin_Lin

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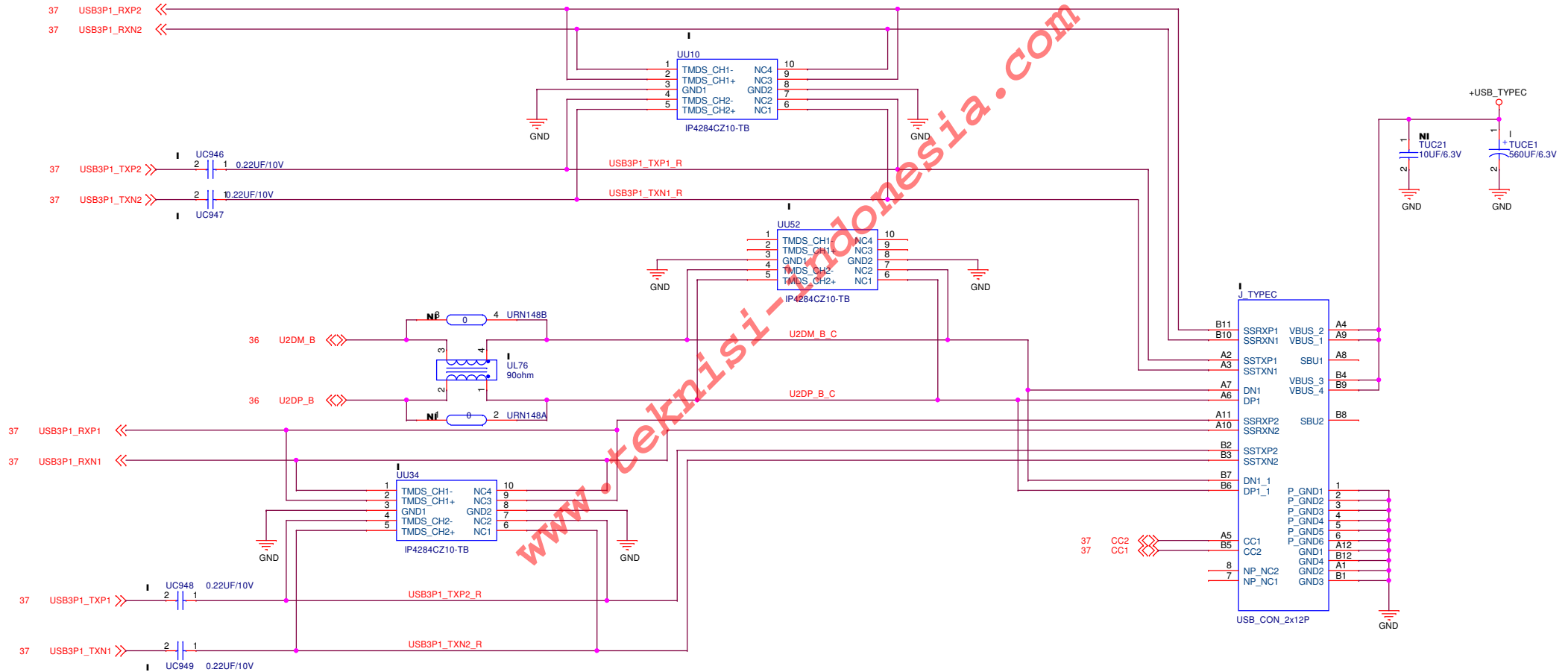


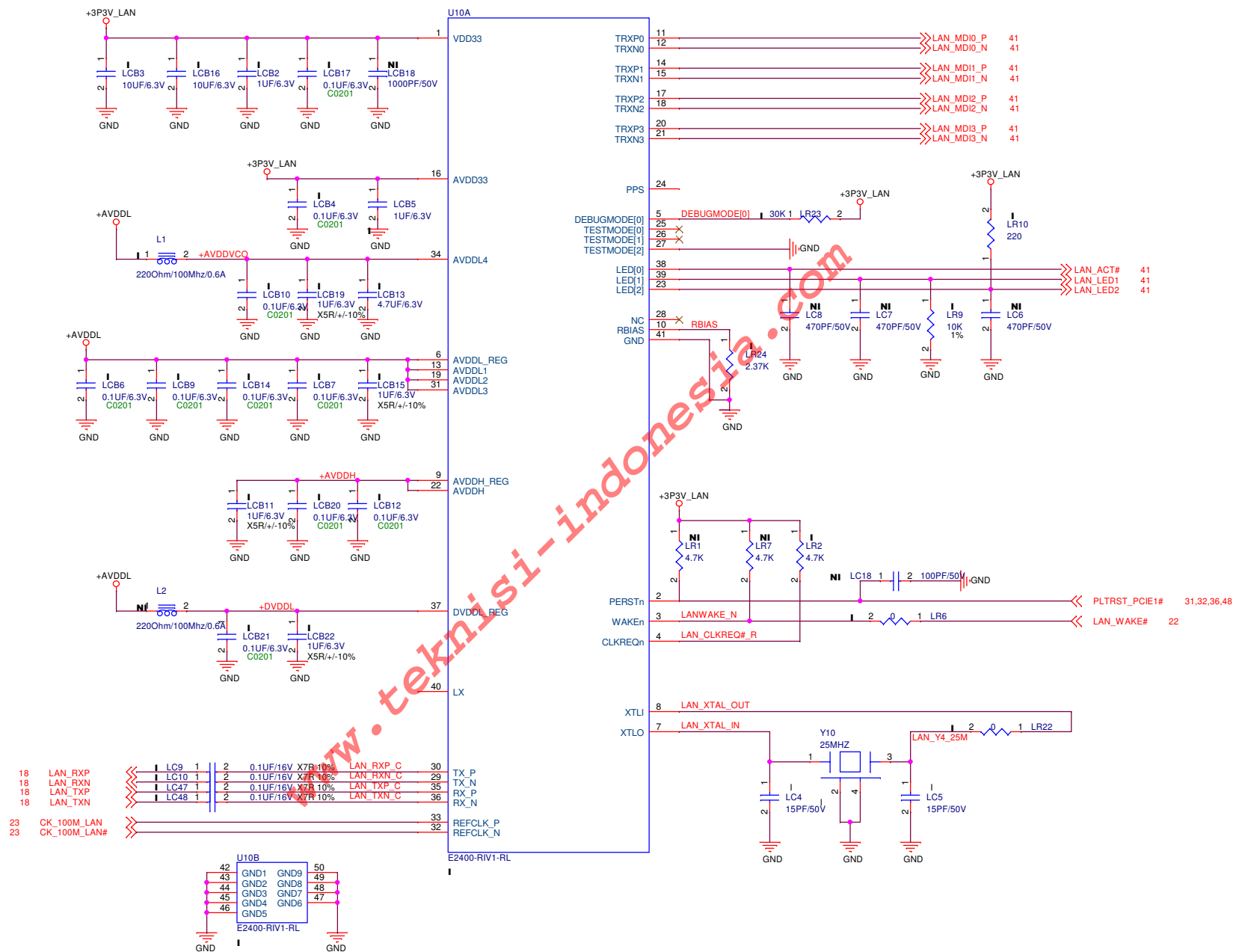


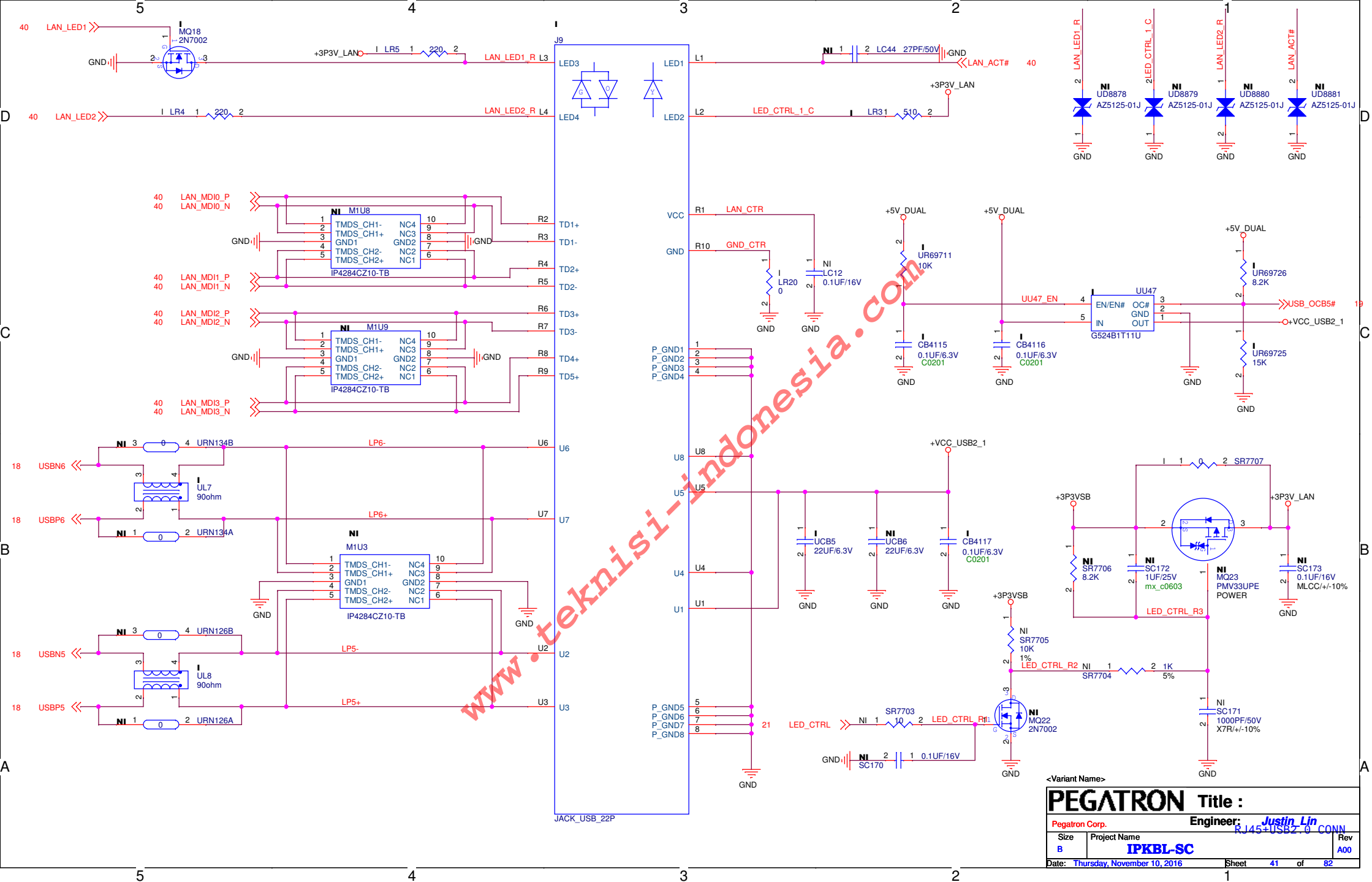
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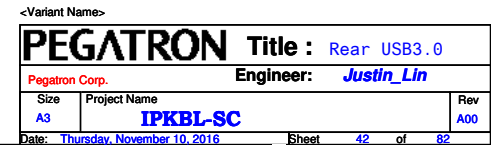
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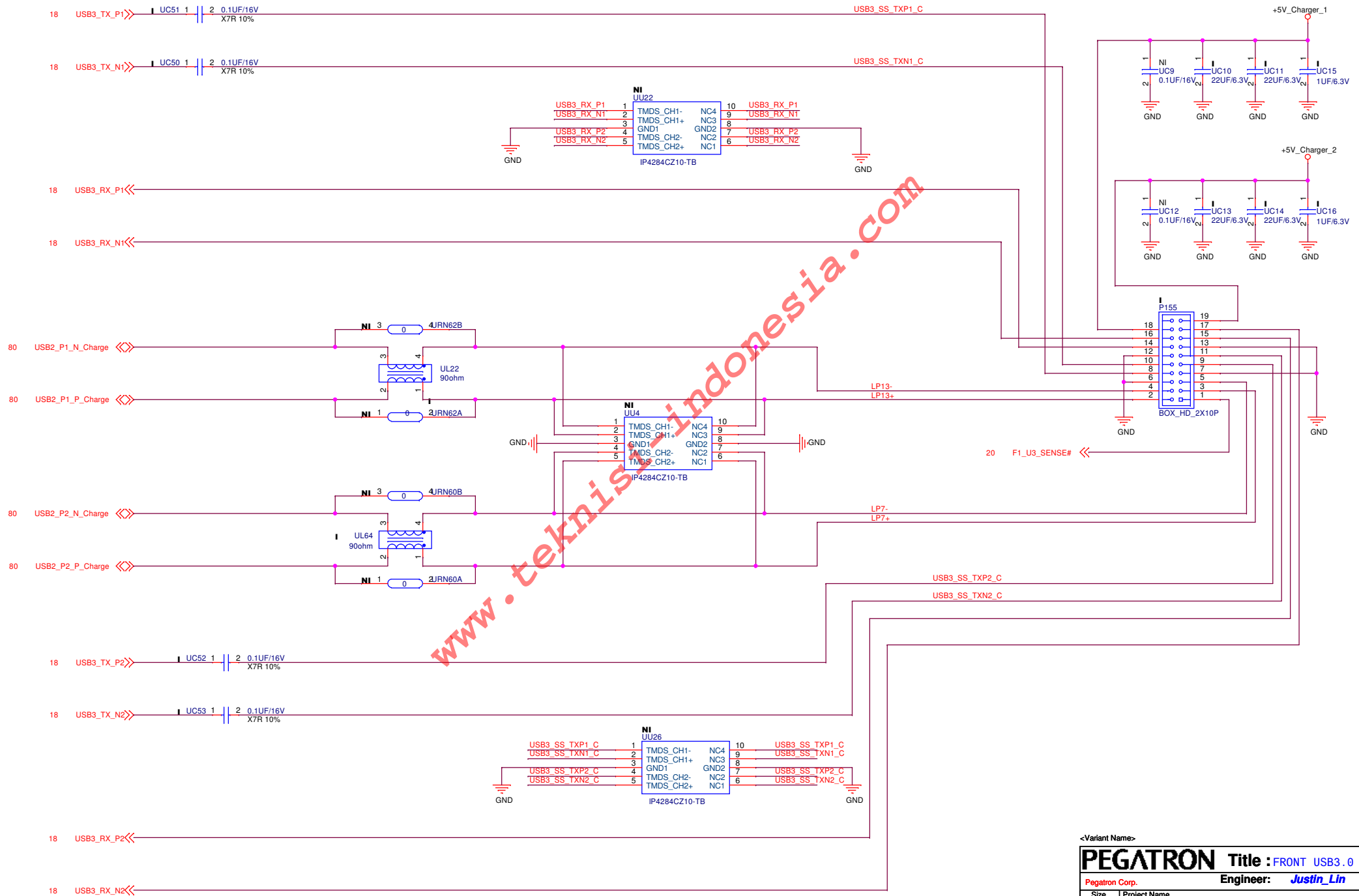
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GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND



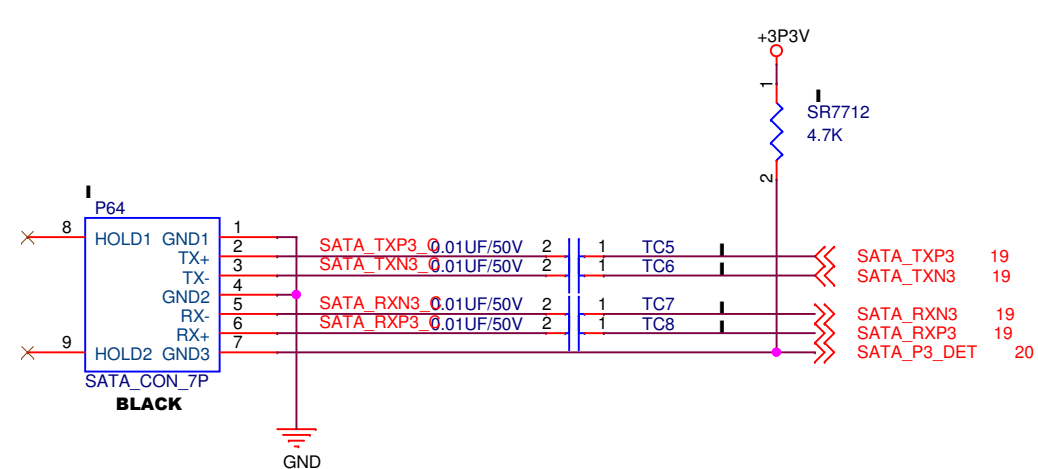
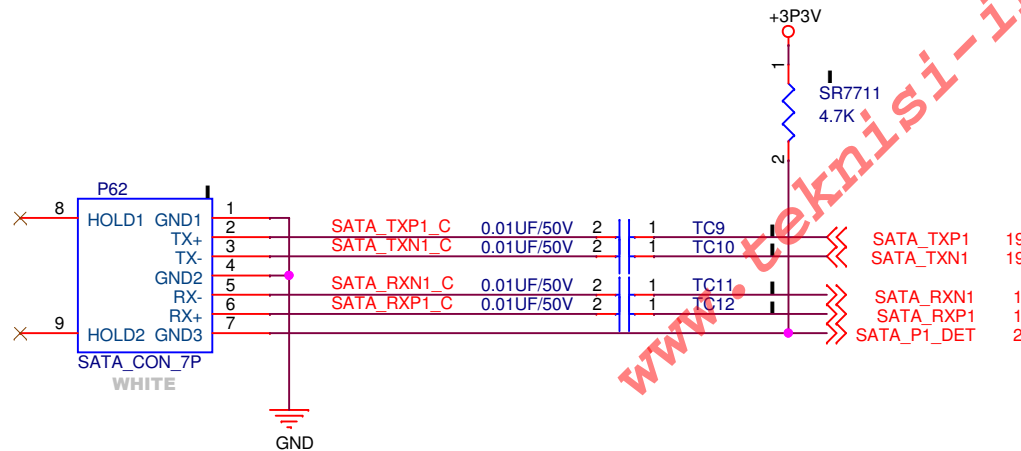
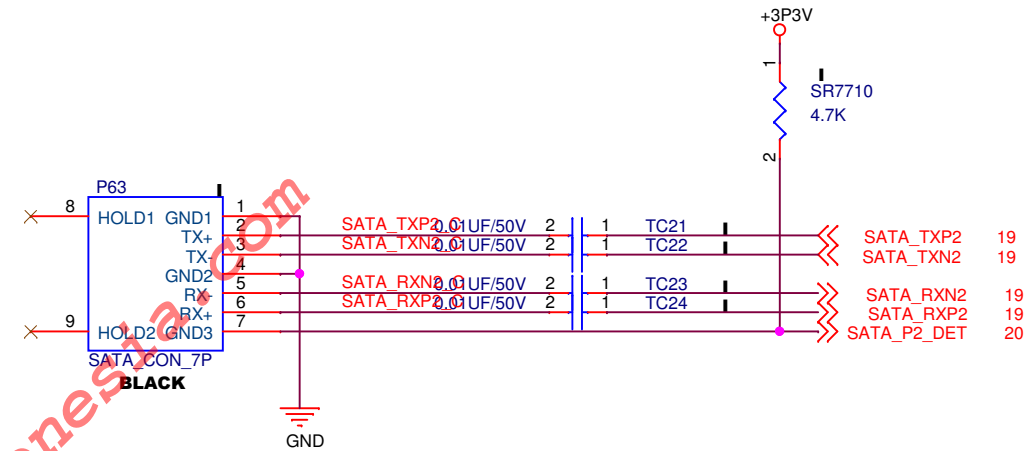
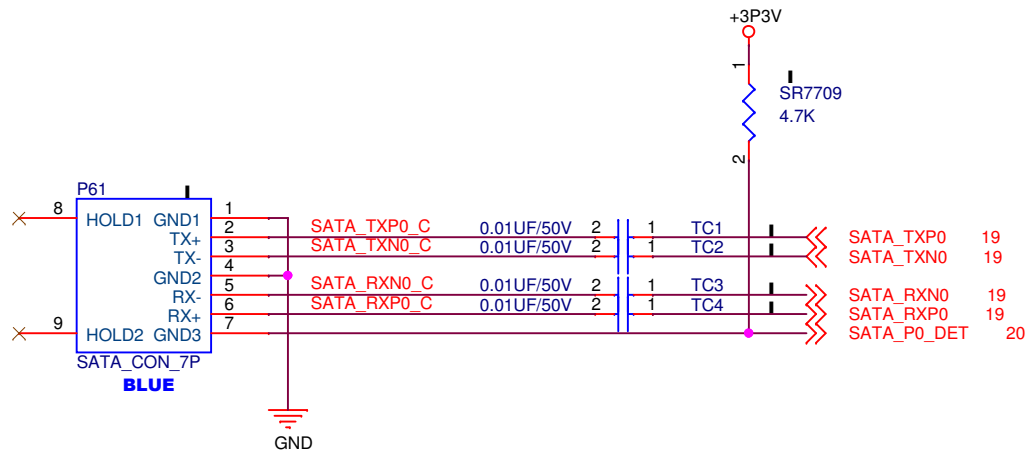




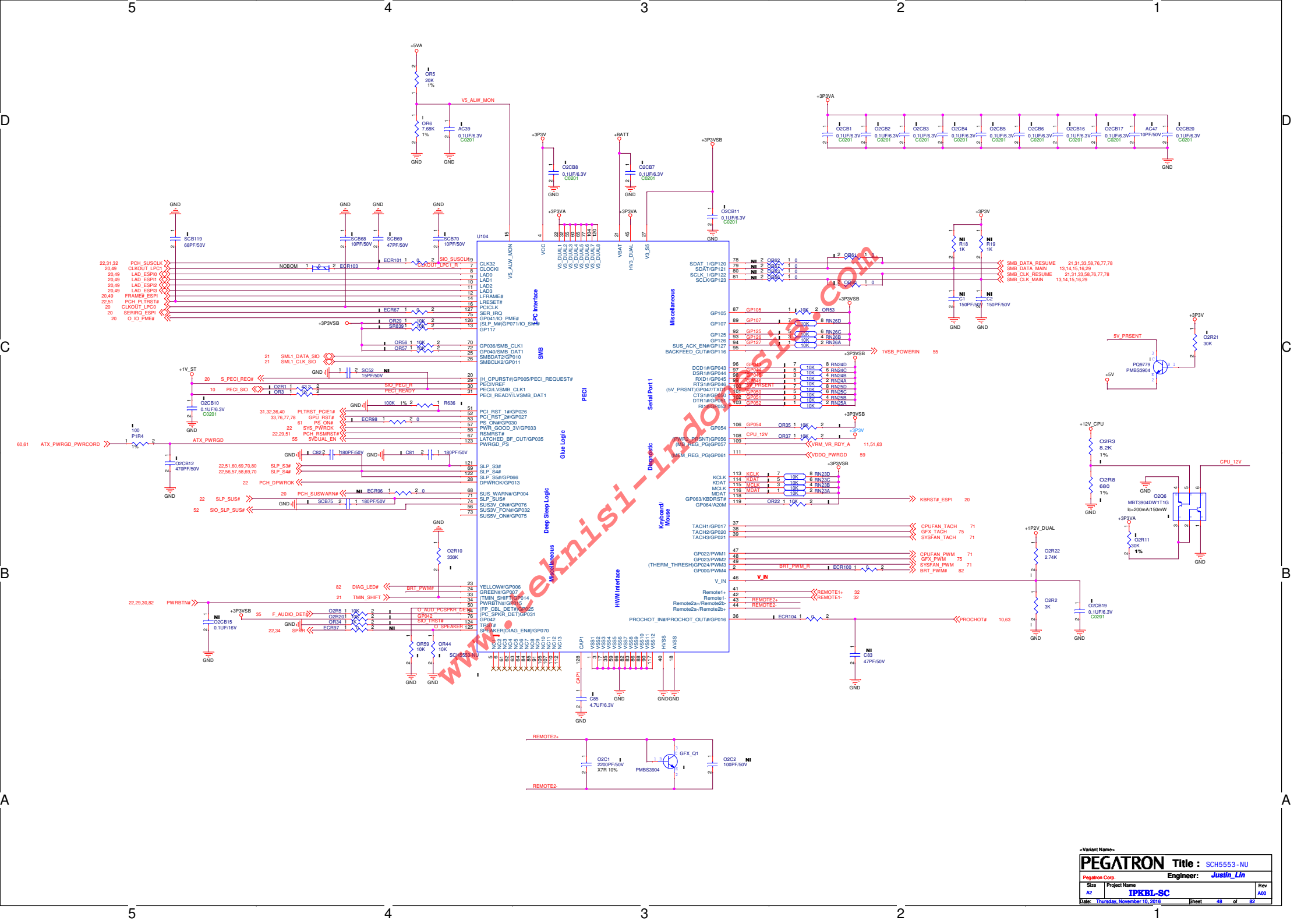


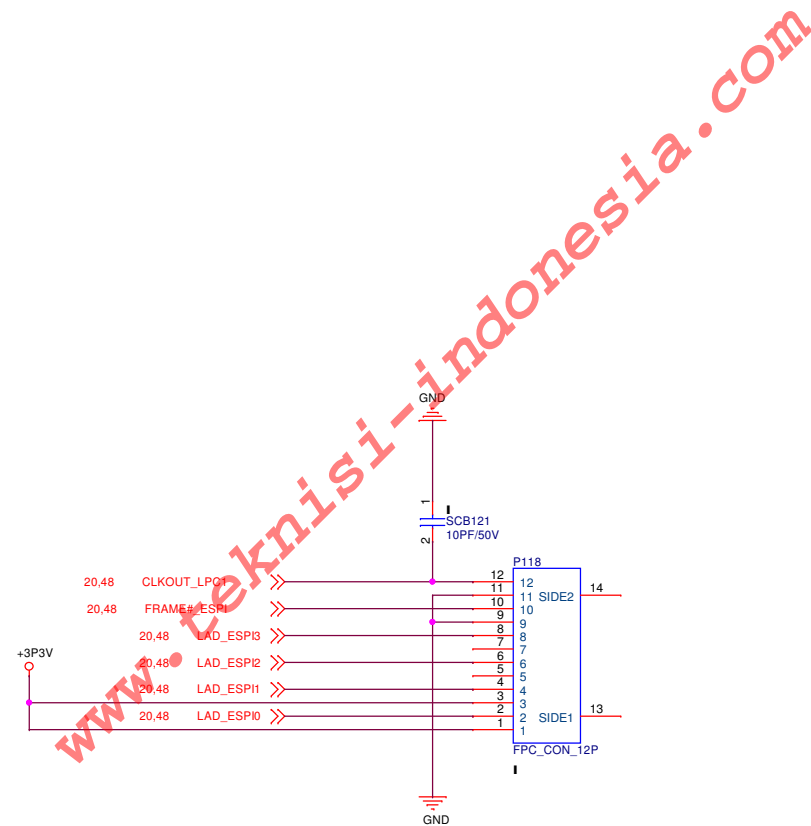


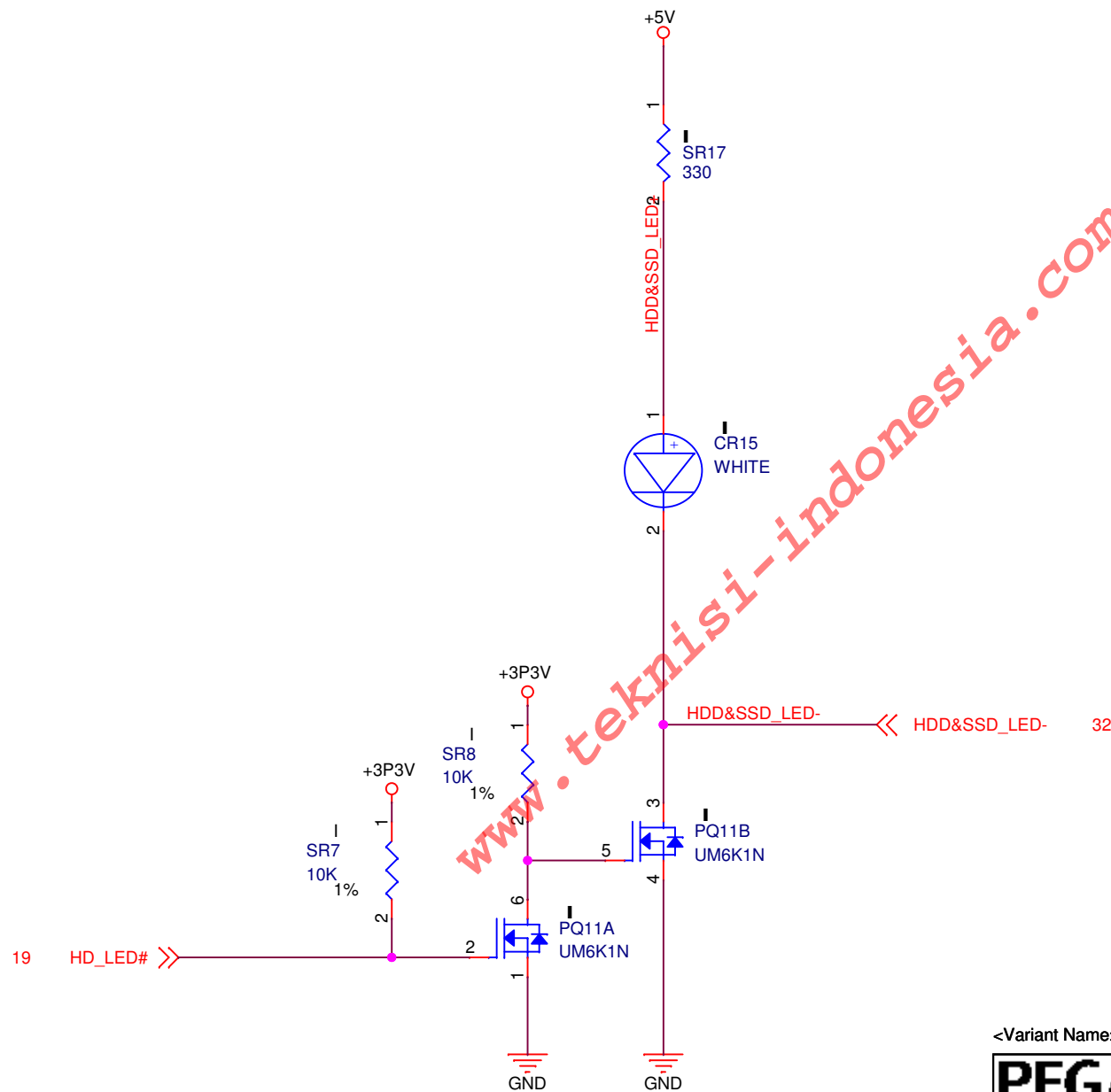
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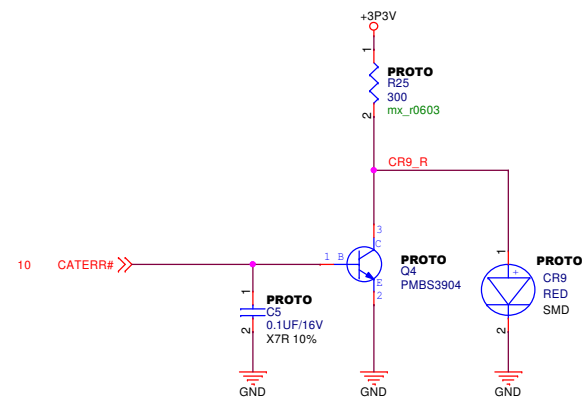
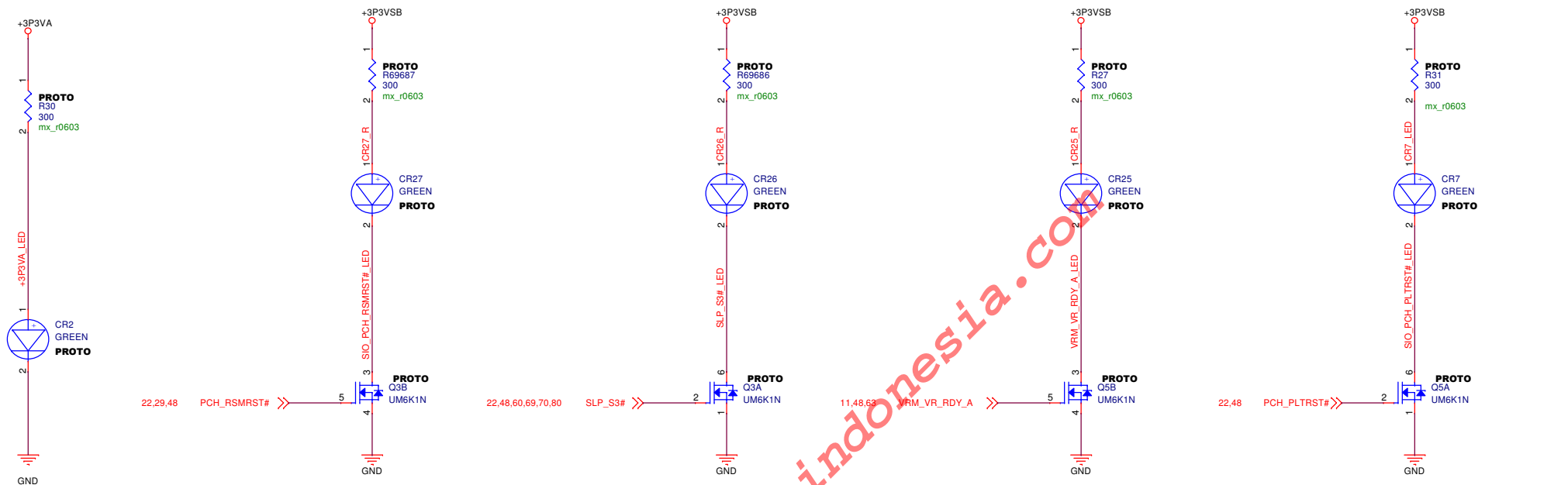


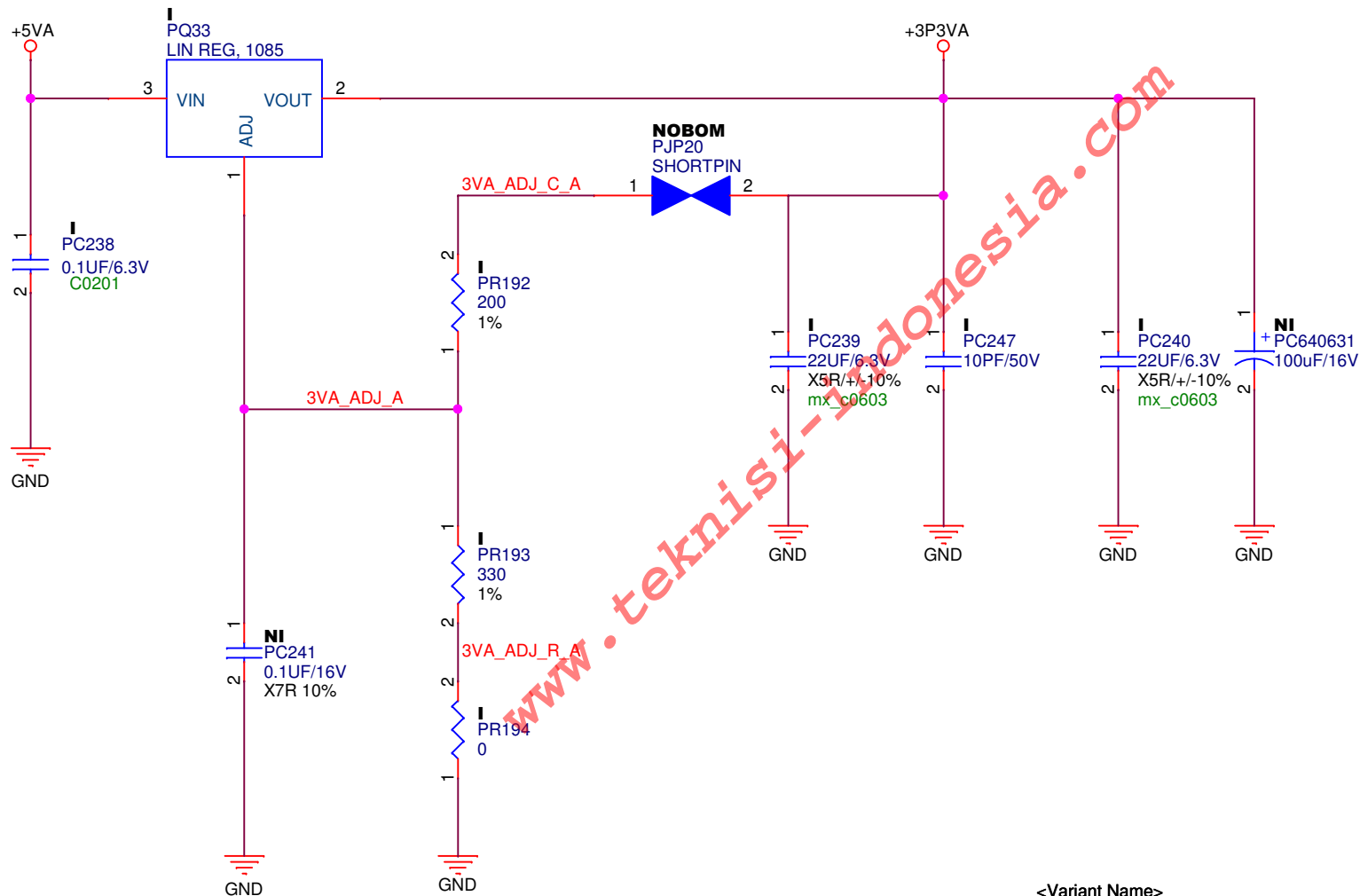


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PEGATRON		Title :	
Pegatron Corp.		Engineer: <i>Justin_Lin</i>	
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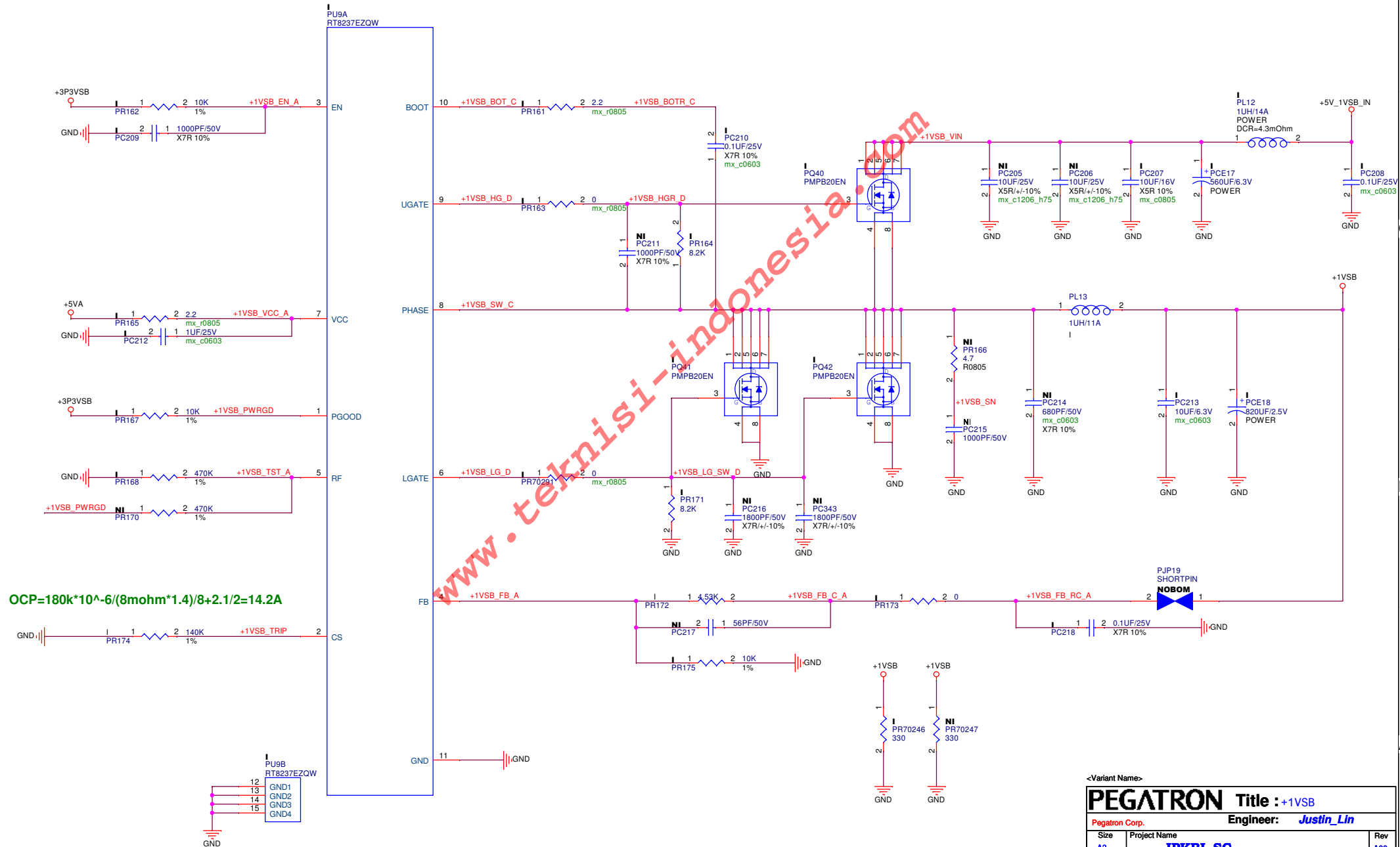


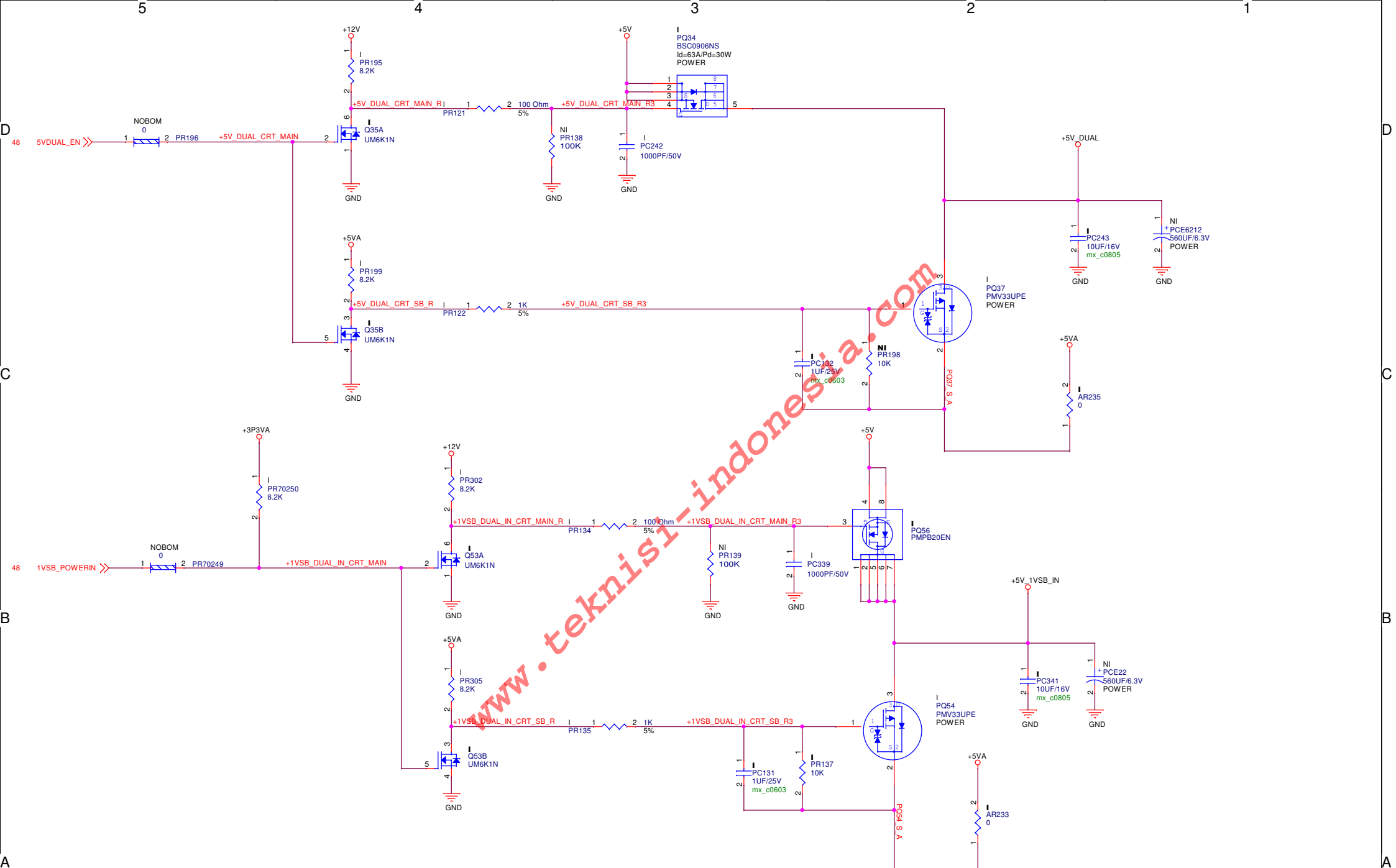
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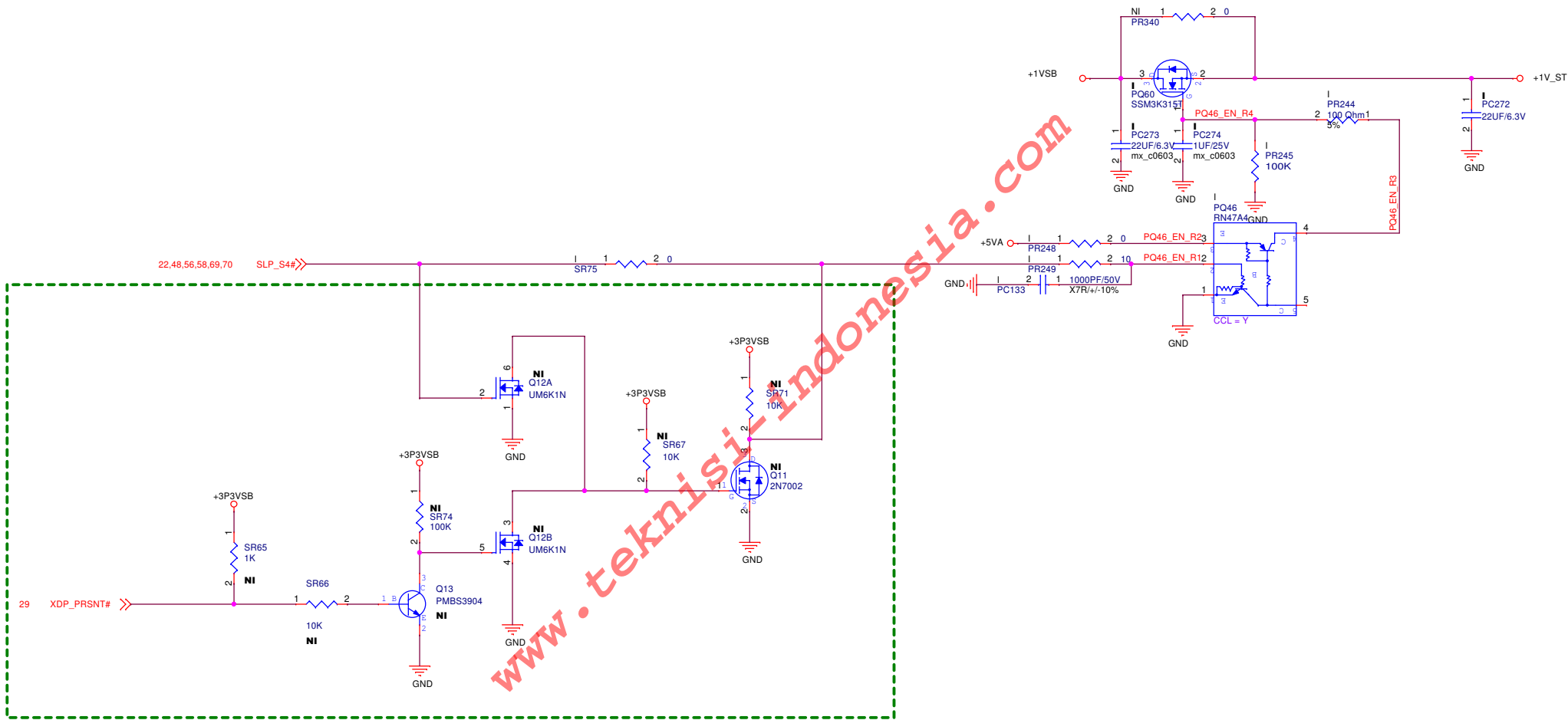
PEGATRON		Title : +3P3VA
Pegatron Corp.		Engineer: Justin_Lin
Size A	Project Name IPKBL-SC	Rev A00
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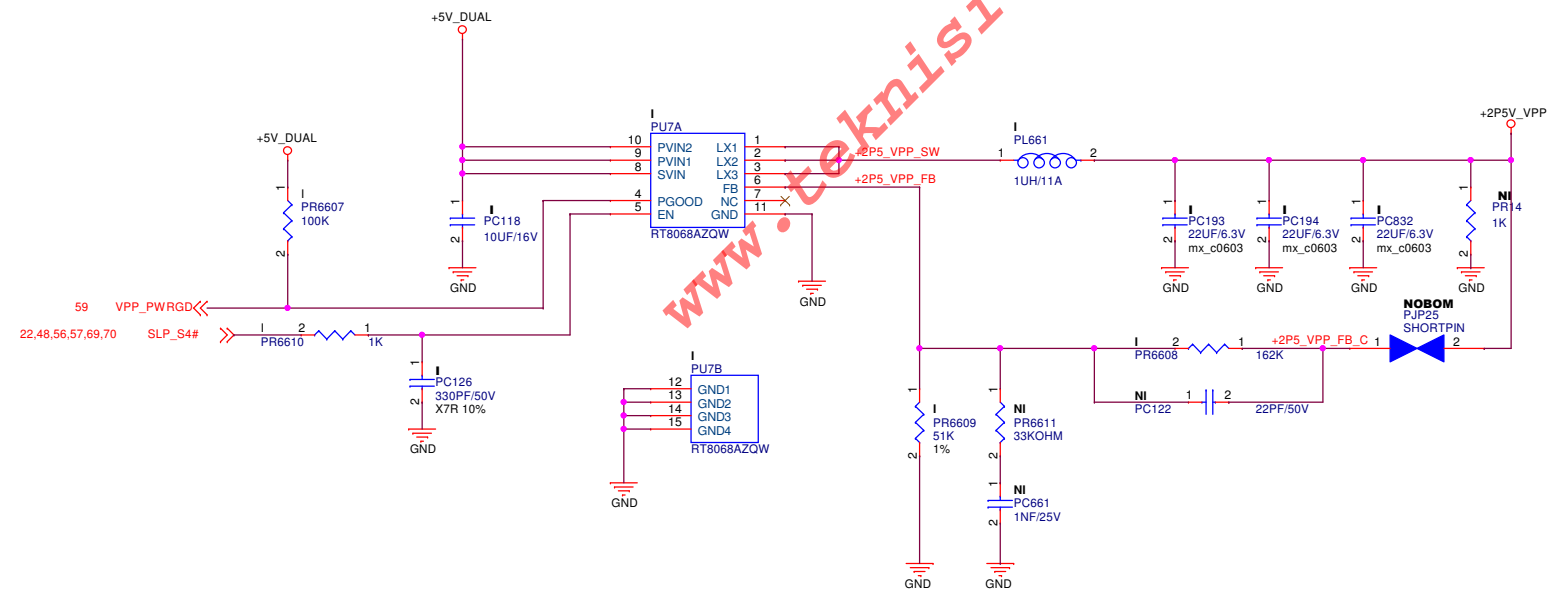
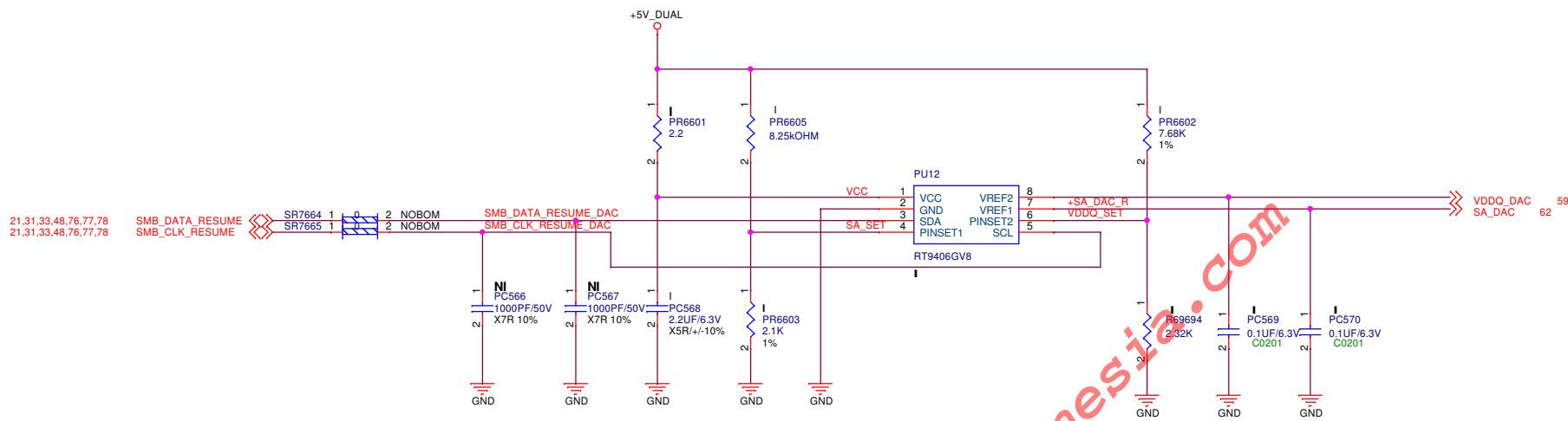
R_{RF} (k Ω)	Switching Frequency (kHz)
470k Ω	290
200k Ω	340
100k Ω	380
39k Ω	430

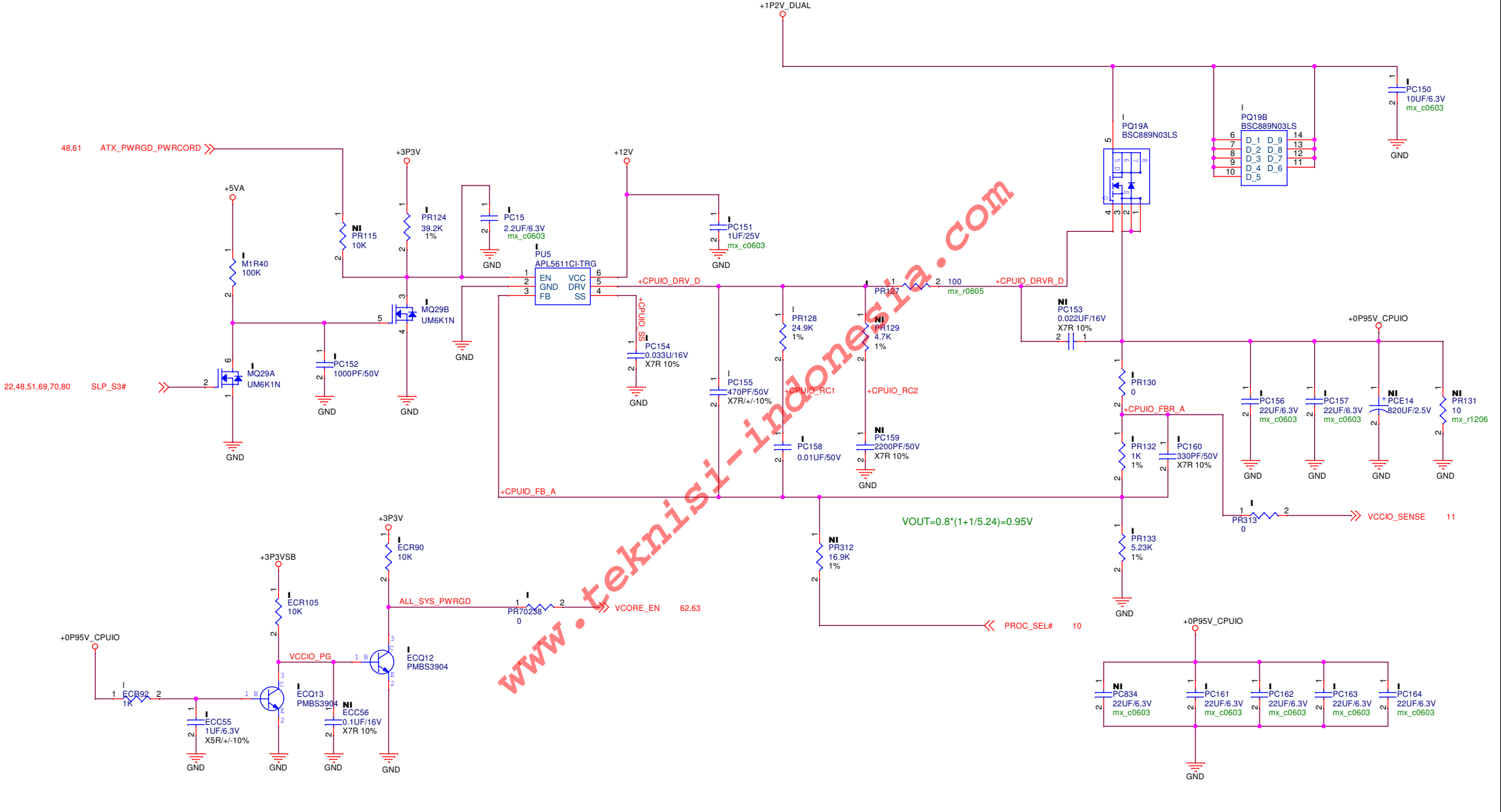
Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.

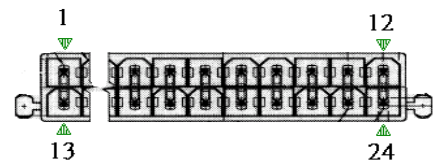




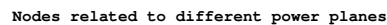








A diagram showing a 2x2 grid of cells. Each cell contains a small black rectangle representing a vehicle. Green arrows with numbers indicate flow directions: 1 (top-left to top-right), 2 (top-right to top-left), 3 (bottom-left to bottom-right), and 4 (bottom-right to bottom-left).



+12V_CPU

For EMI request 2016.10.4

P1CB13 22UF/6.3V

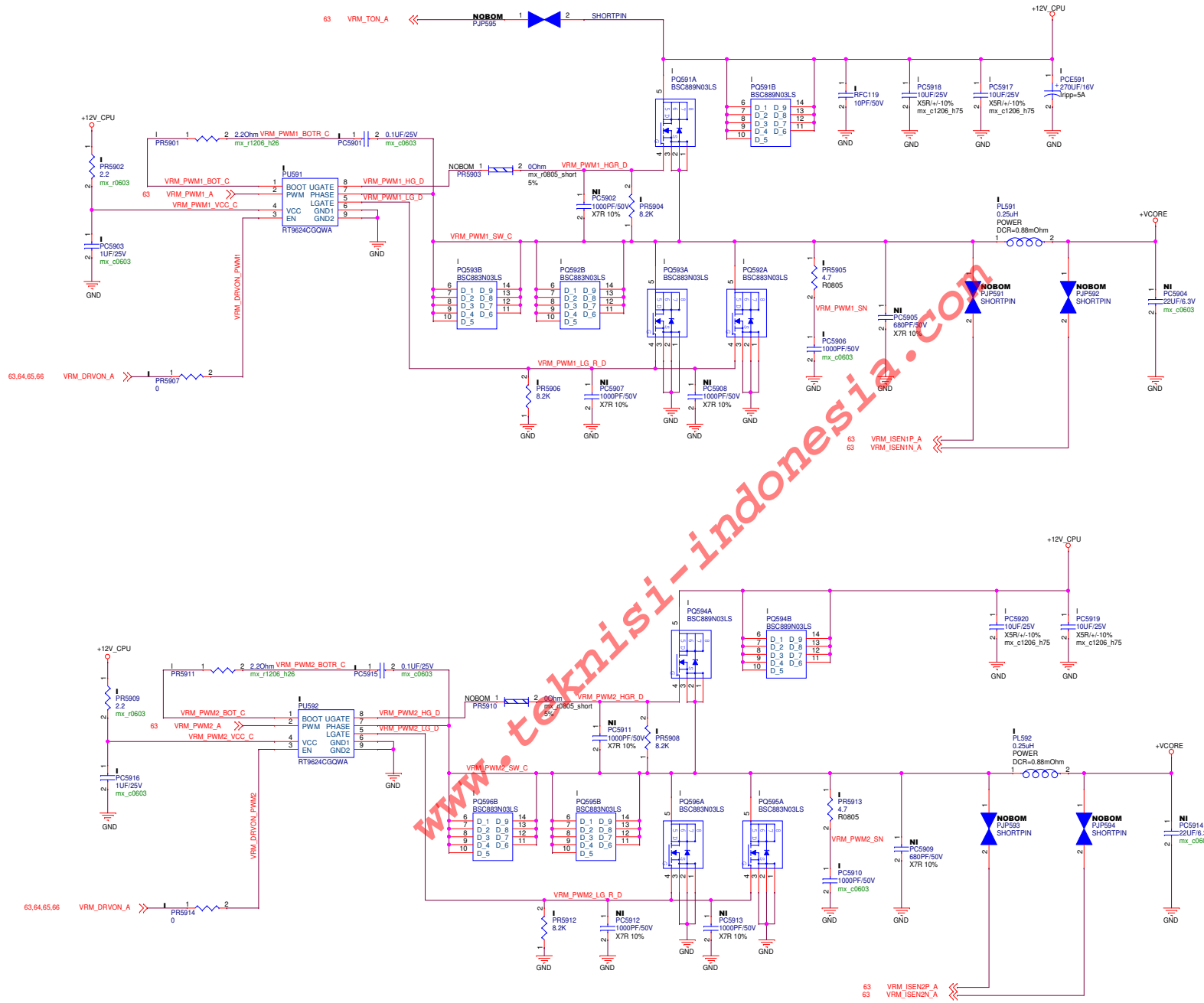
P1CB14 22UF/6.3V

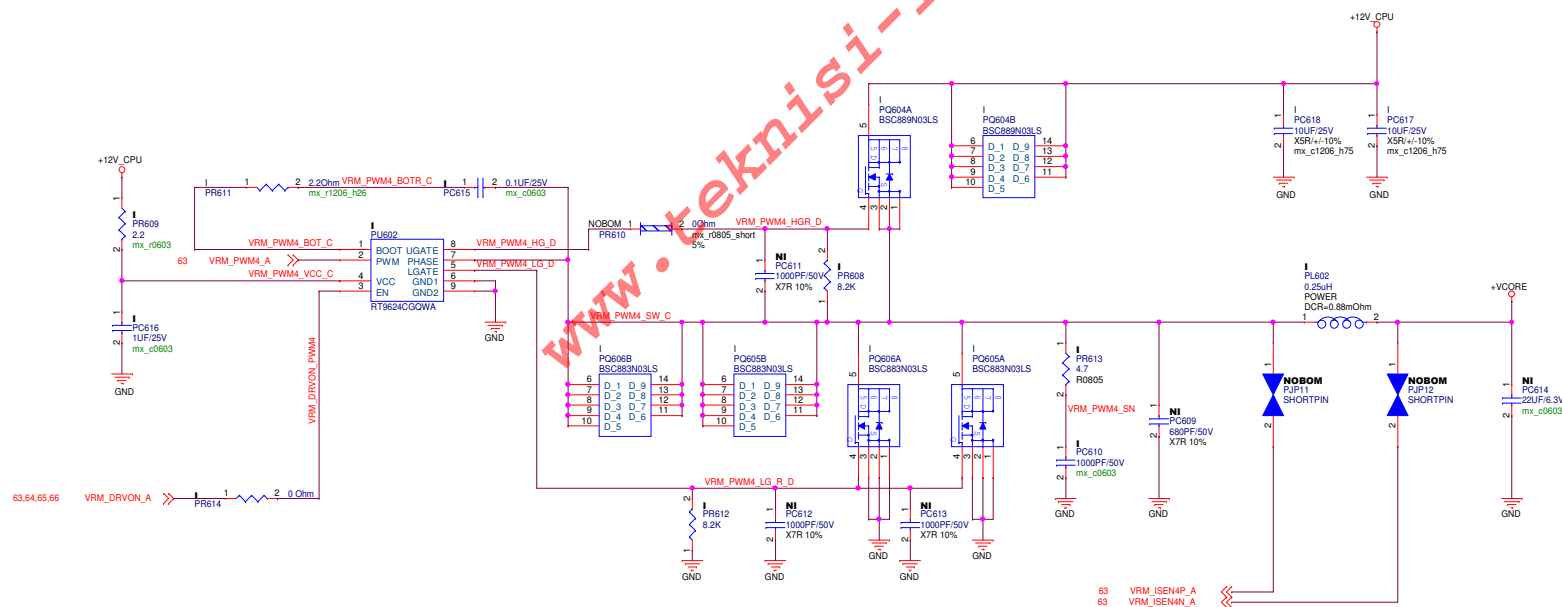
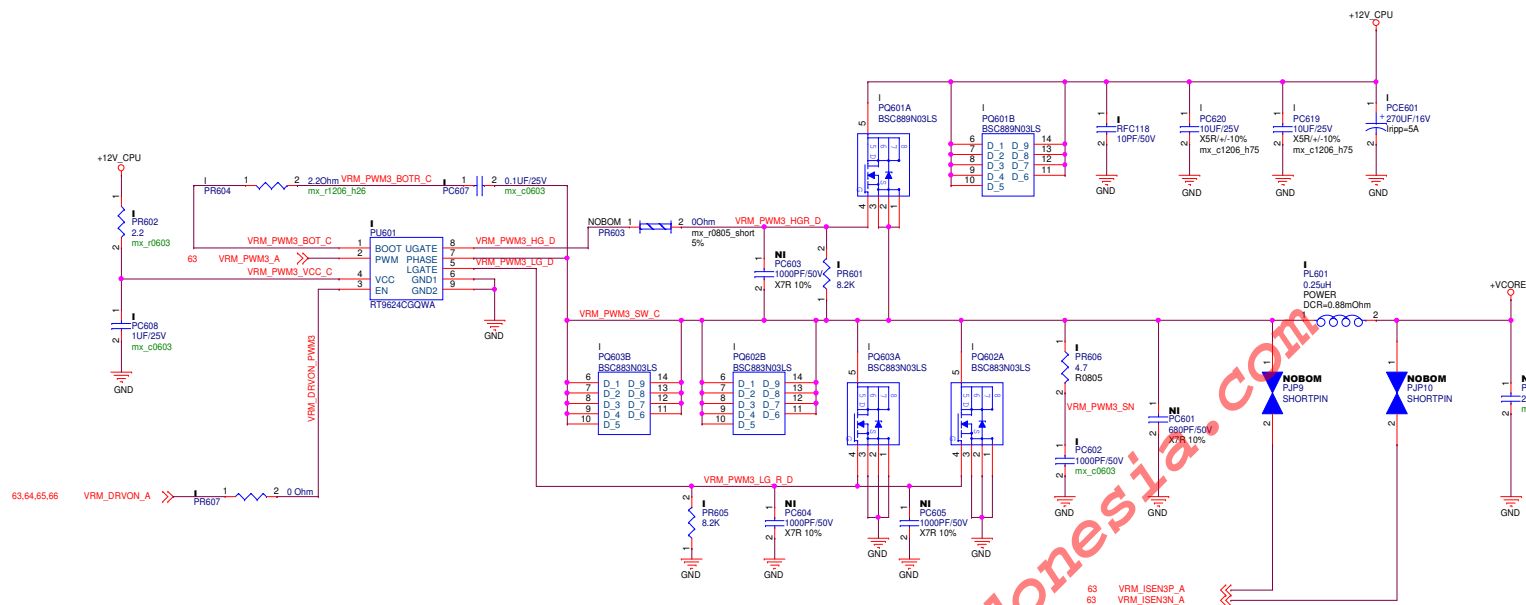
P1CB15 22UF/6.3V

P1CB16 22UF/6.3V

GND

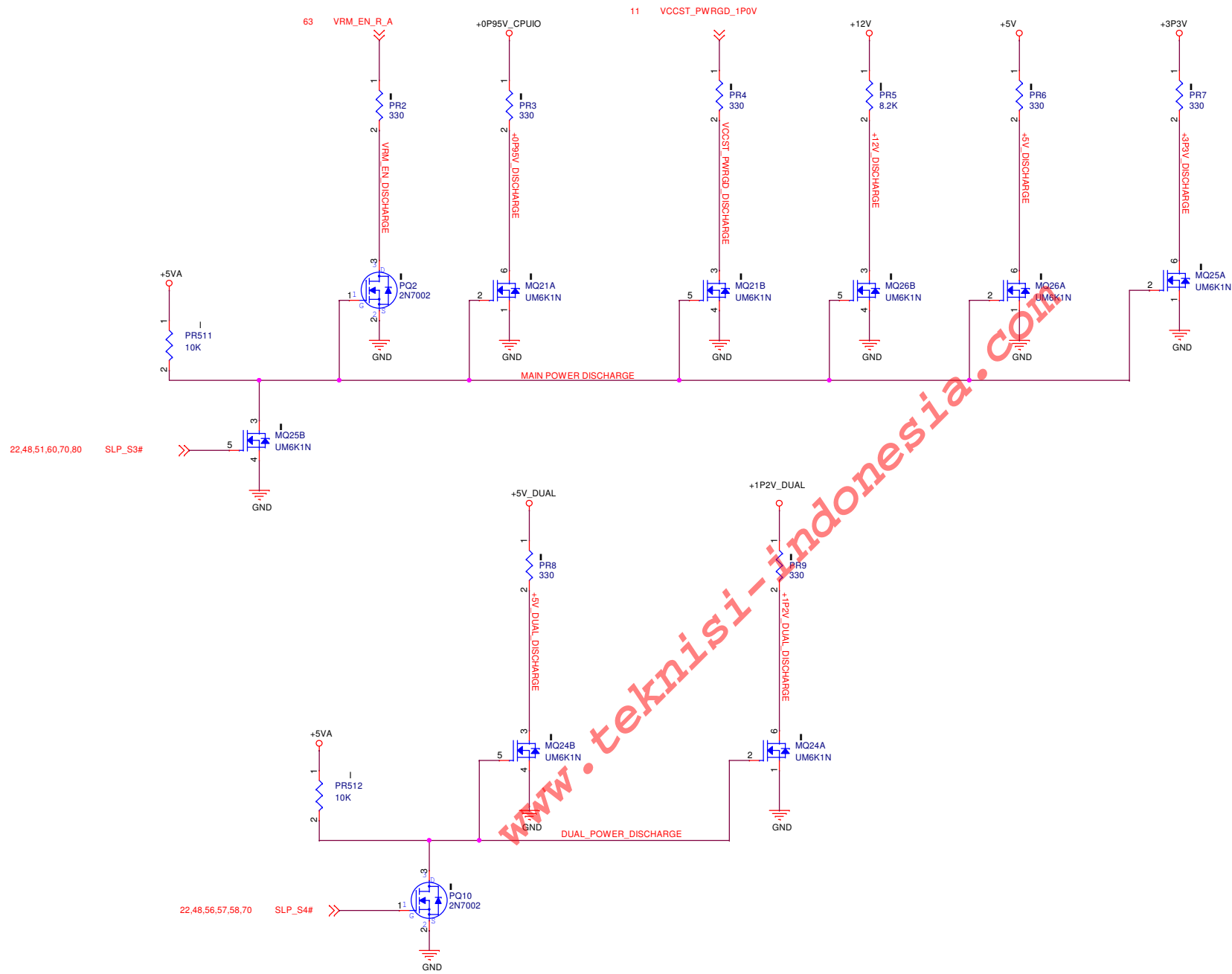
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~Variant Name~

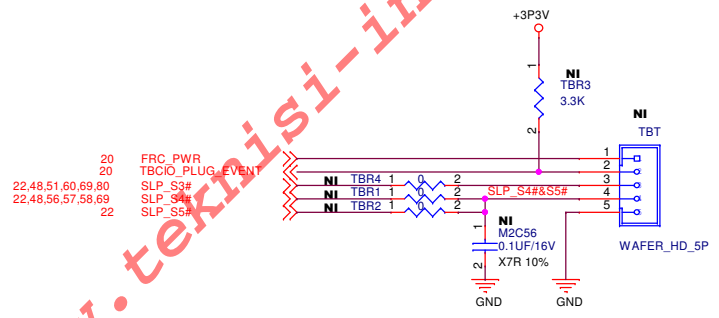
PEGATRON Title :			Engineer: Justin Lin
Size	Project Name	Rev	
C	IPKBL-SC	A00	
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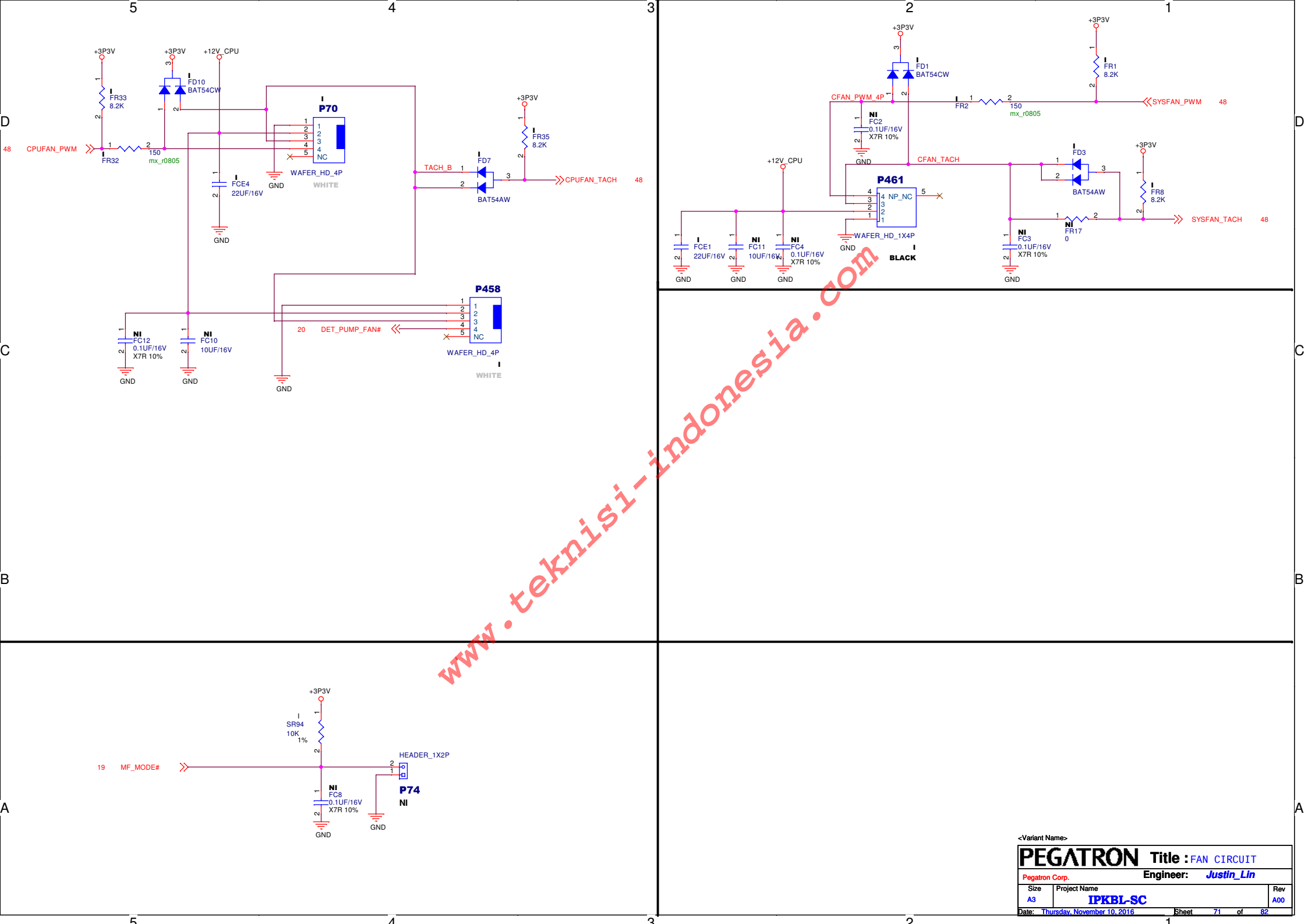


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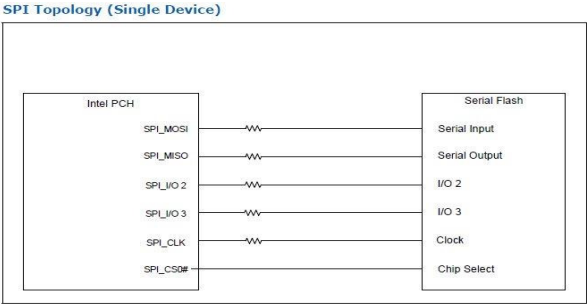
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Pegatron Corp.		Engineer: Justin_Lin	
Size A3	Project Name IPKBL-SC		Rev A00
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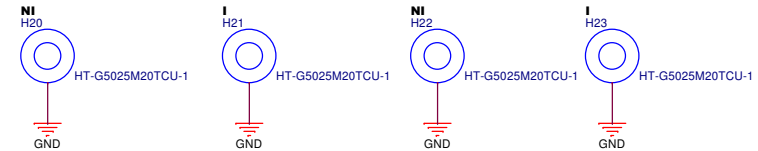
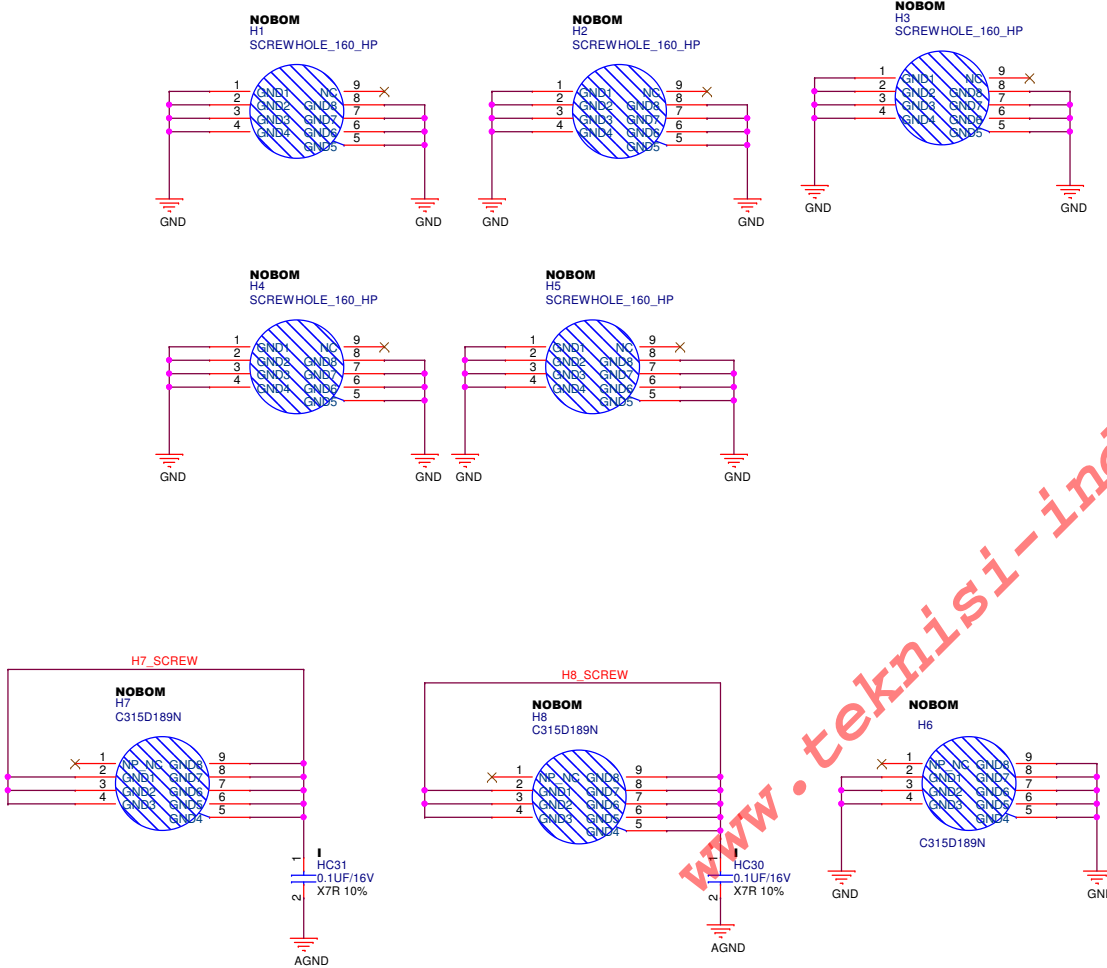


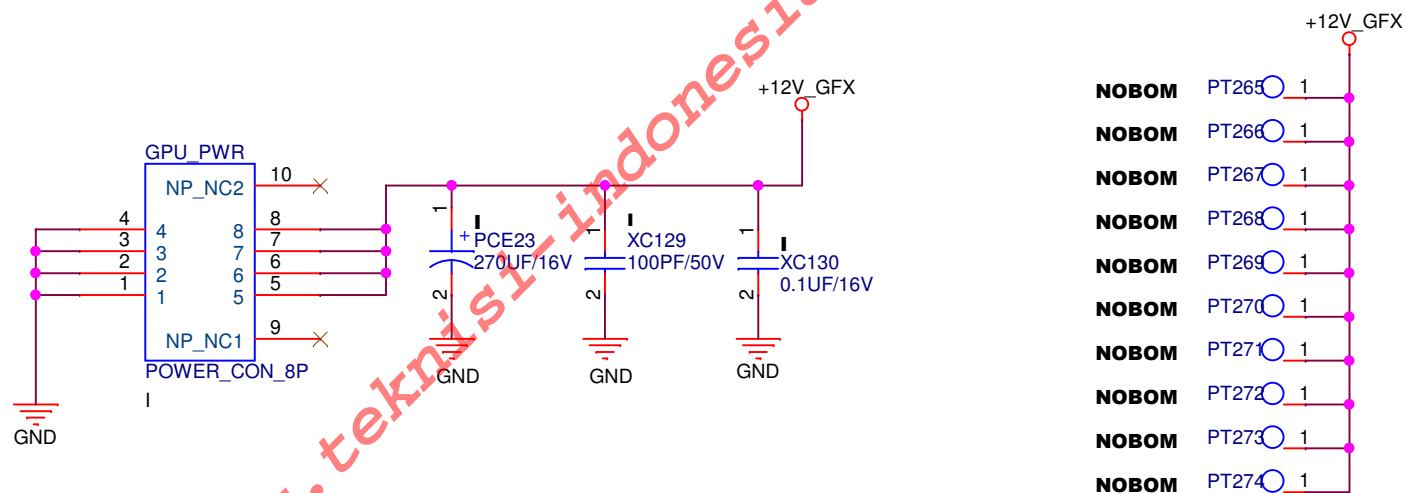
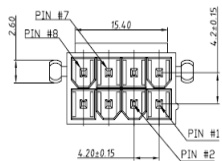


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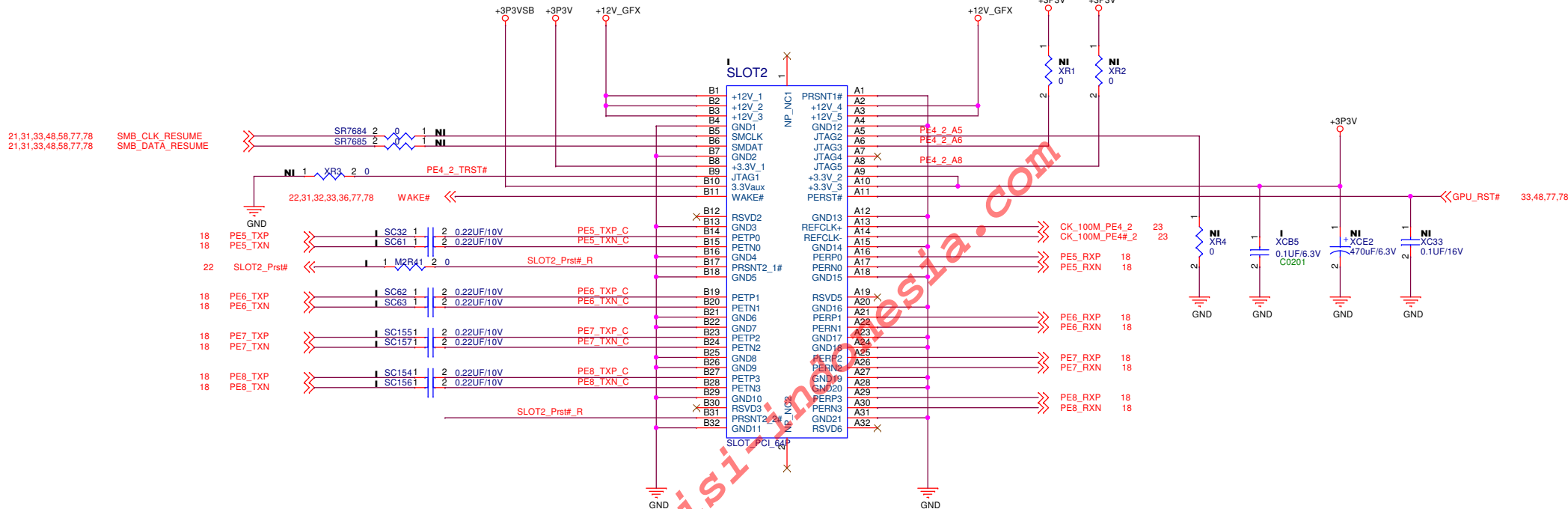
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Pegatron Corp.		Engineer: Justin_Lin	
Size	Project Name		Rev
B	IPKBL-SC		A00
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<Variant Name>

PEGATRON		Title : GPU_PWR	
Pegatron Corp.		Engineer: Justin_Lin	
Size A	Project Name IPKBL-SC		Rev A00
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<Variant Name>

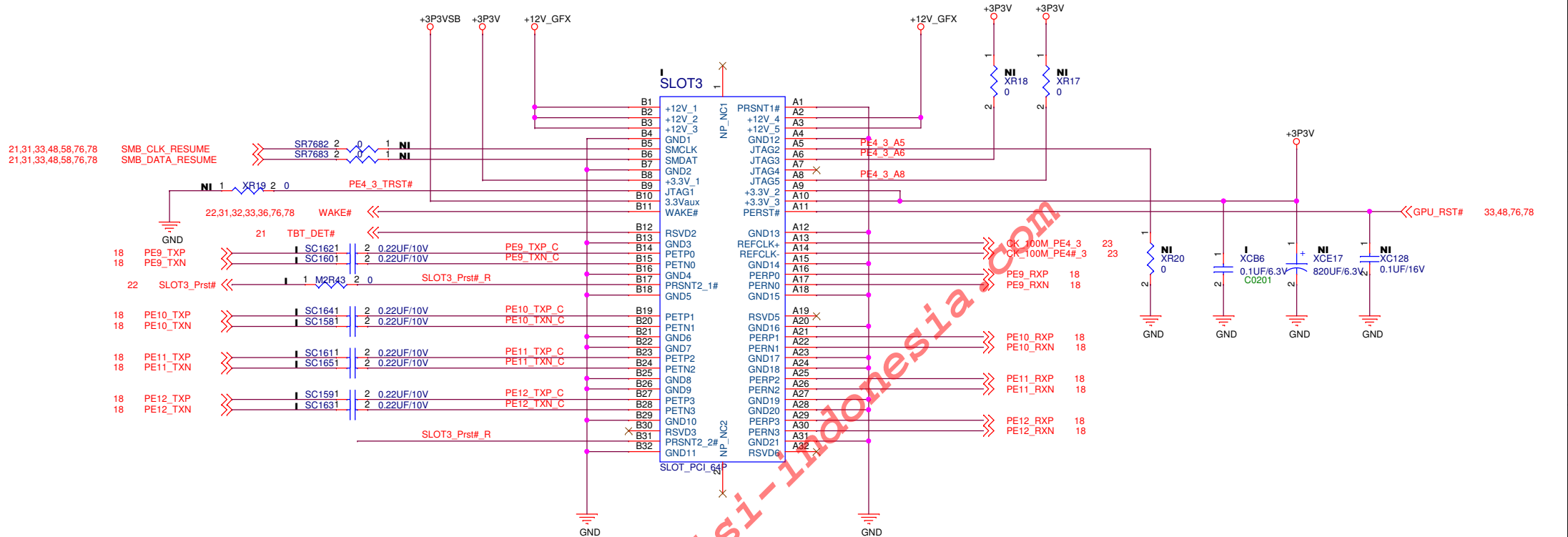
PEGATRON

Title : PCI-E X4 SLOT 2

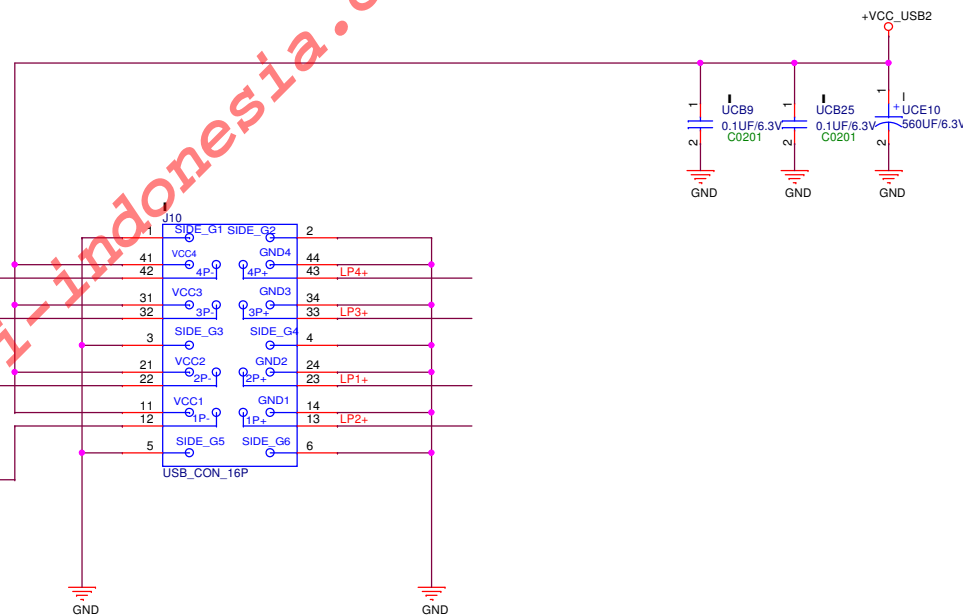
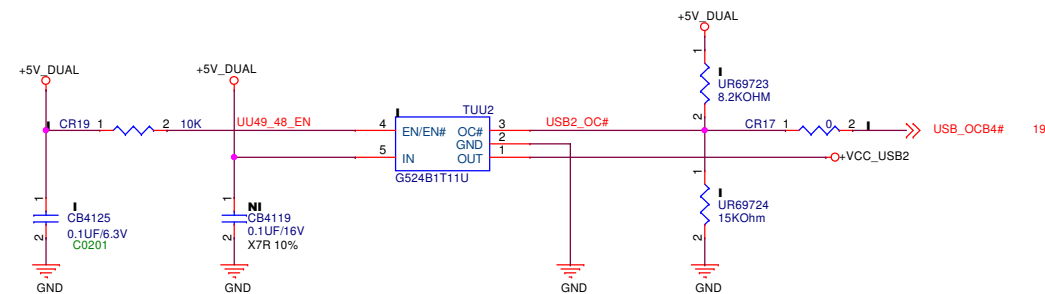
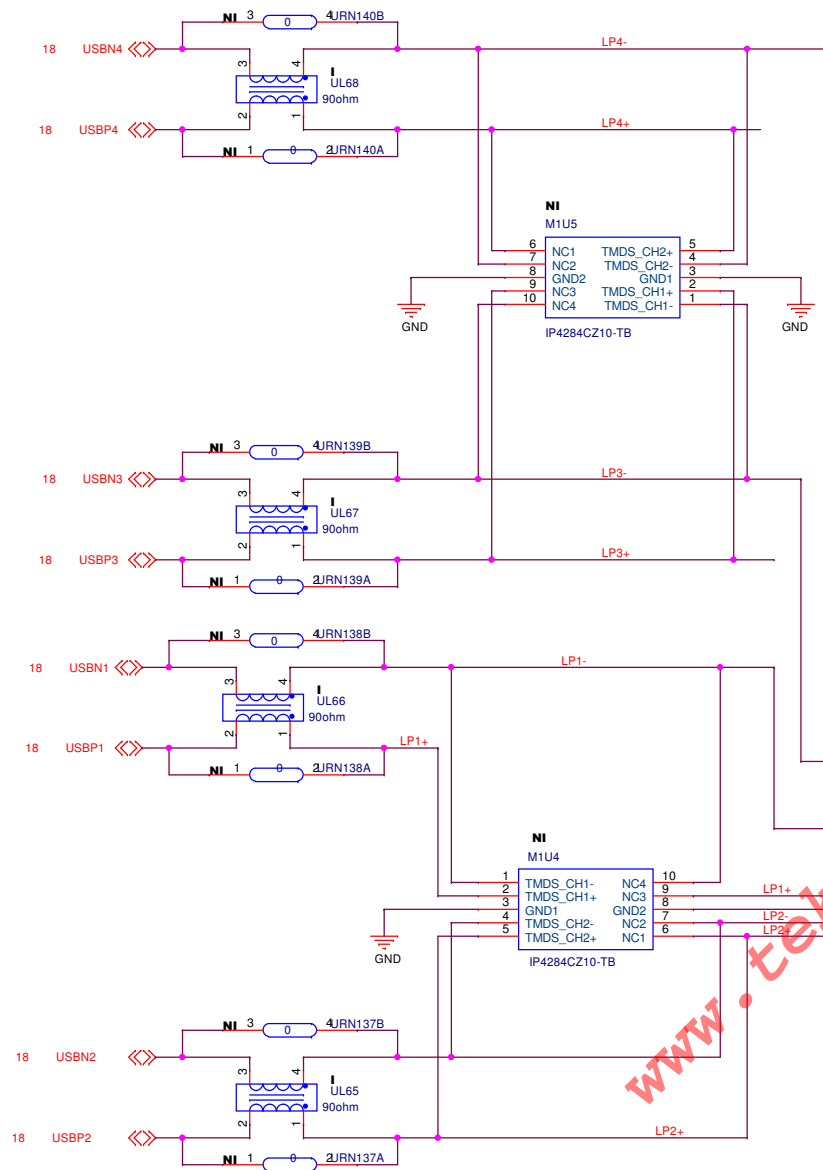
Pegatron Corp.

Engineer: Justin_Lin

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<Variant Name>			
PEGATRON		Title :PCI-E X4 SLOT 3	
Pegatron Corp.		Engineer: Justin_Lin	
Size B	Project Name IPKBL-SC		Rev A00
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<Variant Name>

